Advanced Etch Technology for Nanopatterning

Ying Zhang
Gottlieb Oehrlein
Qinghuang Lin
Editors

13–14 February 2012
San Jose, California, United States

Sponsored and Published by
SPIE

Volume 8328
## Contents

<table>
<thead>
<tr>
<th>Page</th>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>vii</td>
<td>Conference Committee</td>
</tr>
<tr>
<td>ix</td>
<td>Introduction</td>
</tr>
</tbody>
</table>

### SESSION 1 OVERVIEW OF NANOPATTERNING CHALLENGES AND OPPORTUNITIES

8328 03 **Advanced plasma etch technologies for nanopatterning (Keynote Paper)** [8328-02]
R. Wise, IBM Semiconductor Research and Development Ctr. (United States)

8328 04 **Ultimate top-down processes for future nanoscale devices (Invited Paper)** [8328-07]
S. Samukawa, Tohoku Univ. (Japan)

### SESSION 2 NANOPATTERNING FOR ADVANCED TECHNOLOGY NODES

8328 09 **Patterning enhancement techniques by reactive ion etch (Invited Paper)** [8328-06]
M. Honda, Tokyo Electron Miyagi Ltd. (Japan); K. Yatsuda, Tokyo Electron Ltd. (Japan)

8328 0A **Plasma etch transfer of self-assembled polymer patterns (Invited Paper)** [8328-08]
D. E. Johnston, M. Lu, C. T. Black, Brookhaven National Lab. (United States)

8328 0B **Patterning of CMOS device structures for 40-80nm pitches and beyond (Invited Paper)** [8328-09]
S. U. Engelmann, R. Martin, R. L. Bruce, H. Miyazoe, N. C. M. Fuller, W. S. Graham, E. M. Sikorski, M. Glodde, M. Brink, H. Tsai, J. Bucciglano, D. Klaus, E. Kratschmer, M. A. Guillorn, IBM Thomas J. Watson Research Ctr. (United States)

8328 0C **Plasma etch challenges for porous low-k materials for 32nm and beyond (Invited Paper)** [8328-10]
C. Labelle, R. Srivastava, GLOBALFOUNDRIES Inc. (United States); Y. Yin, IBM Corp. (United States); T. Chen, R. Koshy, GLOBALFOUNDRIES, Inc., (United States); Y. Mignot, STMicroelectronics (United States); J. Arnold, D. Horak, IBM Corp. (United States)

8328 0D **Towards new plasma technologies for 22nm gate etch processes and beyond (Invited Paper)** [8328-11]
O. Joubert, M. Darron, G. Cunne, E. Pargone, Lab. des technologies of the Microélectronique, CNRS (France) and Univ. Joseph Fourier (France) and CEA, LETI, MINATEC (France); D. Thibault, CEA, LETI, MINATEC (France); C. Petit-Etienne, L. Vallier, Lab. des technologies of the Microélectronique, CNRS (France) and Univ. Joseph Fourier (France) and CEA, LETI, MINATEC (France); N. Posseme, CEA, LETI, MINATEC (France); P. Bodart, L. Azarnouche, R. Blanc, M. Haas, M. Brihoum, Lab. des technologies de la Microélectronique, CNRS (France) and Univ. Joseph Fourier (France) and CEA, LETI, MINATEC (France); S. Banna, T. Lill, Applied Materials, Inc. (United States)

8328 0F **Etch challenges for 1xnm NAND flash (Invited Paper)** [8328-13]
M. K. Ahn, W. J. Kwon, C. S. Hyun, J. W. Kim, Hynix Semiconductor Inc. (Korea, Republic of)
SESSION 3 PLASMA AND PHOTORESIST INTERACTIONS

8328 0H Plasma treatment to improve linewidth roughness during gate patterning (Invited Paper) [8328-15]
L. Azarnouche, STMicroelectronics (France); E. Pargon, K. Menguelti, M. Fouchier, M. Brihoum, R. Ramos, O. Joubert, Lab. des technologies de la Microélectronique, CNRS (France) and Univ. Joseph Fourier (France) and CEA, LETI, MINATEC (France); P. Gouraud, C. Verove, STMicroelectronics (France)

8328 0I The effects of plasma exposure on low-k dielectric materials (Invited Paper) [8328-16]
J. L. Shohet, H. Ren, M. T. Nichols, H. Sinha, W. Lu, K. Mavrakakis, Univ. of Wisconsin-Madison (United States); Q. Lin, IBM Watson Research Ctr. (United States); N. M. Russell, M. Tomoyasu, Tokyo Electron Ltd. (United States); G. A. Antonelli, Novellus Systems, Inc. (United States); S. U. Engelmann, N. C. Fuller, IBM Watson Research Ctr. (United States); V. Ryan, GLOBALFOUNDRIES Inc. (United States); Y. Nishi, Stanford Univ. (United States)

8328 0J Photoresist strip challenges for advanced lithography at 20nm technology node and beyond (Invited Paper) [8328-17]
I. L. Berry III, C. Waldfried, D. Roh, S. Luo, D. Mattson, J. DeLuca, O. Escorcia, Axxelis Technologies, Inc. (United States)

8328 0L Dry etching challenges for patterning smooth lines: LWR reduction of extreme ultra violet photo resist [8328-19]
E. Altamirano-Sánchez, A. Vaglio Pret, R. Gronheid, W. Boullart, IMEC (Belgium)

8328 0M Self-assembly patterning using block copolymer for advanced CMOS technology: optimisation of plasma etching process [8328-20]
T. Chevolleau, G. Cunje, M. Delalande, Lab. des technologies de la Microélectronique, CNRS (France) and CEA, LETI (France); X. Chevalier, Arkema S.A. (France); R. Tiron, CEA, LETI, MINATEC (France); S. David, M. Daron, Lab. des technologies de la Microélectronique, CNRS (France) and CEA, LETI (France); C. Navarro, Arkema S.A. (France)

8328 0N EUV resist curing technique for LWR reduction and etch selectivity enhancement [8328-21]
K. Narishige, T. Katsumuma, M. Honda, Tokyo Electron Miyagi Ltd. (Japan); K. Yatsuda, Tokyo Electron Ltd. (Japan)

8328 0O Mandrel and spacer engineering based self-aligned triple patterning [8328-22]
Y. Chen, Q. Cheng, W. Kang, Peking Univ. (China)

8328 0P Transfer optimized dry development process of sub-32nm HSQ/AR3 BLR resist pillar from low-K etcher to metal etcher [8328-23]

POSTER SESSION

8328 0Q How much further can lithography process windows be improved? [8328-24]
M. A. Hockey, Q. Lin, E. Calderas, Brewer Science, Inc. (United States)

8328 OS Pattern transfer from the e-beam resist, over the nanoimprint resist and to the final silicon substrate [8328-27] J. He, GeSiM Gesellschaft für Silizium-Mikrosysteme mbH (Germany) and Technical Univ. Dresden (Germany); S. Howitz, GeSiM Gesellschaft für Silizium-Mikrosysteme mbH (Germany); K. Richter, J. W. Bartha, Technische Univ. Dresden (Germany); J. I. Moench, Leibniz-Institut für Festkörper- und Werkstoffforschung Dresden (Germany)

8328 OT Exploration of suitable dry etch technologies for directed self-assembly [8328-26] F. Yamashita, E. Nishimura, Tokyo Electron Miyagi Ltd. (Japan); K. Yatsuda, H. Mochiki, Tokyo Electron Ltd. (Japan); J. Bannister, Tokyo Electron America, Inc. (United States)


8328 OV 3d modeling of LER transfer from the resist to the underlying substrate: the effect of the resist roughness [8328-29] G. Kokkoris, V. Constantoudis, E. Gogolides, National Ctr. for Scientific Research Demokritos (Greece)

Author Index
Conference Committee

Symposium Chairs

Donis G. Flagello, Nikon Research Corporation of America (United States)
Harry J. Levinson, GLOBALFOUNDRIES Inc. (United States)

Conference Chair

Ying Zhang, Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)

Conference Co chairs

Gottlieb Oehrlein, University of Maryland, College Park (United States)
Qinghuang Lin, IBM Thomas J. Watson Research Center (United States)

Program Committee

Julie Bannister, Tokyo Electron America, Inc. (United States)
Maxime Darnon, Laboratoire des technologies de la Microélectronique, CNRS (France)
Sebastian U. Engelmann, IBM Thomas J. Watson Research Center (United States)
Eric A. Hudson, Lam Research Corporation (United States)
Catherine B. Labeille, GLOBALFOUNDRIES Inc. (United States)
Nae-Eung Lee, Sungkyunkwan University (Korea, Republic of)
Denis Shamiryan, GLOBALFOUNDRIES Dresden Module Two, GmbH & Company KG (Germany)
Jeffrey J. Xu, Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)
Anthony Yen, Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)

Session Chairs

1 Overview of Nanopatterning Challenges and Opportunities
Ying Zhang, Taiwan Semiconductor Manufacturing Company Ltd. (Taiwan)
Catherine B. Labelle, GLOBALFOUNDRIES Inc. (United States)
2 Nanopatterning for Advanced Technology Nodes
Gottlieb S. Oehrlein, University of Maryland, College Park (United States)
Sebastian U. Engelmann, IBM Thomas J. Watson Research Center (United States)

3 Plasma and Photoresist Interactions
Qinghuang Lin, IBM Thomas J. Watson Research Center (United States)
Julie Bannister, Tokyo Electron America, Inc. (United States)
Introduction

The success of the semiconductor industry has been enabled by the relentless pursuit of technological innovations. The continuous strive to improve device features, enhance performance and simultaneously reduce manufacturing costs is incessant. While optical lithography has traditionally been the major driving force to advance technology, new materials and enhanced synergy between fabrication technologies have become increasingly important for the development of manufacturing at advanced-technology nodes. One such area of increased importance involves plasma etch and related patterning technology. While plasma etch has always been an integral part of semiconductor technology, it has significantly grown in importance with the emergence of Double Patterning and Pitch-Splitting (DP/PS) technology for 22nm technology node and beyond.

Recent advances in lithographic technology include 193-nm immersion optical lithography, EUV lithography, Multi-e-Beam Direct Writing (MEBDW), and alternative lithographic technologies, such as directed self-assembly patterning (DSA), and nanoimprint lithography. All of these lithography technologies depend on advancing plasma etch, which is used either directly in the patterning process, such as patterning and forming lithography masks, or in transferring lithographic patterns into other layers, e.g., during multi-litho and multi-etching lithography patterning, which will be most likely used for high-volume manufacturing (HVM) at 22nm technology node and beyond. The increasing interactions and inter-dependence of lithography, photoresist technologies, and plasma etch technologies inevitably makes advancing lithography and plasma etch technologies for semiconductor manufacturing more challenging. This situation is the motivation for having an “Advanced Etch Technology for Nanoaatttering Conference (AETNC)” as a key part of the SPIE Advanced Lithography Symposium starting 2012. This new conference brings lithography and plasma-etching communities together to exchange ideas, share new research and development results, discuss gaps in our fundamental understanding and resolve challenges facing the semiconductor industry.

We aim to establish the AETNC as a premier and influential conference on plasma etch technology in the semiconductor industry and to complement the technical programs of other conferences at the SPIE Advanced Lithography Symposium. The first AETNC featured papers from major integrated device manufacturers (IDM’s), foundries, key tool vendors, research institutes, national labs, and universities from around the world. These papers covered all key aspects related to plasma etching for advanced patterning technologies for Logic and Memory products, FEOL applications (such as the formation of 3D device structures of FinFET, BEOL challenges and possible solutions line-edge roughness (LER) for a variety of resists, e.g., 193i, EUV, e-beam resists, etc.), wet etch, resist stripping, and UV treatment/processing. Topics related to key emerging technologies for
nanopatterning, such as directed self-assembly (DSA), were also presented during the conference.

This proceedings volume collects selected papers presented at the first AETNC, held on February 13–14th, 2012 as part of the SPIE Advanced Lithography Symposium 2012.

We would like to take this opportunity to thank the SPIE 2012 Advanced Lithography Symposium Committee for helping initiate the AETNC. The dedication, enthusiasm, and efforts of many committee members, keynote speakers, invited speakers, and authors of contributed papers of AETNC made this conference success. Please accept our well-deserved thanks!

Ying Zhang
Gottlieb Oehrlein
Qinghuang Lin