International Roadmap for Devices and Systems lithography roadmap

Mark Neisser[a,b,*]
[a]Xiamen University, Tan Kah Kee Innovation Laboratory, Xiang'an Campus, Xiang'an District, Xiamen, China
[b]Xiamen University, School of Electronic Science and Engineering, Haiyun Campus, Xiamen, China

Abstract

Background: Planned improvements in semiconductor chip performance have historically driven improvements in lithography and this is expected to continue in the future. The International Roadmap for Devices and Systems roadmap helps the industry plan for the future.

Aim: The 2021 lithography roadmap shows requirements, possible options, and challenges for the next 15 years.

Results: Critical dimensions in logic chips are now small enough that stochastics, i.e., random variations in photon, molecules, and photoresist image forming processes, introduces random variations in sizes and stochastic-driven defects. As critical dimensions get smaller, stochastics becomes a bigger challenge. The roadmap projects that despite projected improvements in tools, photoresist, device design, and patterning processes, resist dose to print will still have to roughly triple over the next 10 years to maintain acceptable stochastics unless major process or chip design changes are made. This will raise patterning costs substantially. Other patterning options are under development but they also have challenges related to defects. Edge placement error (EPE) is also a challenge for future devices. Long-term, logic device requirements will drive stacked devices, and yield and process complexity will be key challenges.

Conclusions: Logic devices will drive leading edge lithography. Improved extreme ultraviolet lithography is a leading candidate but other options are possible. Key short-term challenges are stochastics, EPE, and cost. Resist dose to print is expected to rise substantially as critical dimensions shrink unless substantial process innovation occurs. For the long term, the challenges will be yield and process complexity when logic devices switch to 3D scaling

 [DOI: 10.1117/1.JMM.20.4.044601]

Keywords: lithography; roadmap; stochastics; extreme ultraviolet lithography; photo-speed; International Roadmap for Devices and Systems; ITRS; lithography roadmap; photoresist.

Paper 21029 received Apr. 21, 2021; accepted for publication Aug. 20, 2021; published online Oct. 4, 2021.

1 Introduction

The first semiconductor roadmap was perhaps Moore's observation that chip computing power increased exponentially with time.[1,2] This led semiconductor producers to plan for regular chip improvements. The equipment and materials suppliers to those chip producers also needed to have an idea how technology would progress in the future and so the International Technology Roadmap for Semiconductors (ITRS) roadmap for semiconductors was created. Chip manufacturers collaborated and created projections of future needs and challenges to provide a public description of where the industry was going and what it would need. This roadmap has evolved into the International Roadmap for Devices and Systems or IRDS Roadmap.[3] This roadmap

*Address all correspondence to Mark Neisser, mark@neissers.net

differs from the ITRS one in that it is derived more top down than bottom up. Instead of being driven by stated needs of semiconductor producers, it is developed by projecting future progress in device performance and then determining what types of devices and structures will be needed to provide that future performance. It has many sections. This paper focuses on the lithography section of the 2021 update of the lithography roadmap.

2 Requirements

The More Moore section of the IRDS roadmap projects improvements in traditional logic and memory chips. The projected improvements are driven by the need for big data, the internet of things, cloud computing, and general needs for improved performance. It predicts that high-performance logic devices will drive resolution improvement and that dynamic random-access memory (DRAM) devices will trail in resolution to logic. Non-volatile memory has switched to mostly 3D scaling and will not be driving resolution. Projected dimensions for key logic levels are shown in Fig. 1. Dimensions get smaller for the next 10 years and then are predicted to stop shrinking as logic switches to 3D scaling.

Figure 2 shows the projected lithographic requirements for logic and DRAM taken from the 2021 lithography roadmap. Note that the name of the node is in quotation marks because the node name no longer represents an actual physical dimension in any logic product.

Historically, one of the key challenges highlighted by lithography roadmaps has been resolution. Future generations of chips were projected to require better resolution than current lithography systems could provide. This is no longer the case. Extreme ultraviolet lithography (EUV) systems already in manufacturing use can resolve the smallest line and space dimension on the roadmap if double patterning is used. For contact holes and other hole type levels, double exposure with current tools can already resolve the minimum pitch needed until the "1.5 nm" is 2025. The "1.5 nm" node will be doable with double exposure with high NA EUV tools expected to be in use at the time.[4] After that, no further resolution improvements are projected to be needed.

The cells containing resolution data are colored yellow, "manufacturable solutions are known," where double patterning with EUV can already produce that dimension. Where EUV double patterning will not suffice without high NA EUV or where the lithography committee considers the double patterning pattern quality is questionable, the cells are coded red, "manufacturable solutions are not known." The major lithographic challenges in the next 10 years are mostly related to noise and defects. Overlay is also expected to be a challenge.

3 Possible Options

Part of the lithography roadmap is a description of potential solutions to future challenges. These are shown in Figs. 3 and 4 for lines and spaces and for contact holes, respectively. In these figures, the horizontal direction is time and also the minimum CD that needs to be patterned. The rows reflect different logic and memory nodes. The gray bars indicate when a node is

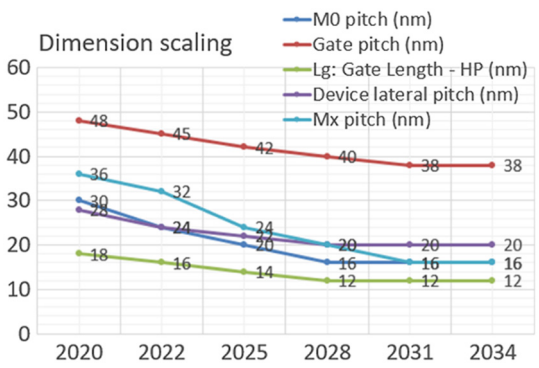

Fig. 1 Projected logic critical dimensions.

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
DRAM							
DRAM minimum ½ pitch (nm)	18	17.5	17	14	11	8.4	7.7
Key DRAM Patterning Challenges	Resolution improvements at reasonable cost						
CD control (3 sigma) (nm) [B]	1.8	1.8	1.7	1.4	1.1	0.84	0.8
Mininum contact/via after etch (nm) [H]	18	17.5	17	14.0	11	8.4	7.7
Minimum contact/via pitch(nm)[H]	54	53	51	42	33	25.2	23
Overlay (3 sigma) (nm) [A]	3.6	3.5	3.4	2.8	2.2	1.68	1.5
MPU / Logic							
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
Key MPU/Logic Patterning Challenges	EPE, Single Exposure for <36nm pitch, Cost of EUV patterning						
MPU/ASIC Minimum Metal ½ pitch (nm)	18	15	12	10	8	8	8
Metal LWR (nm) [C]	2.7	2.3	1.8	1.5	1.2	1.2	1.2
Metal CD control (3 sigma) (nm) [B]	2.7	2.3	1.8	1.5	1.2	1.2	1.2
Contacted poly half pitch (nm)	27.0	24.0	22.5	21.0	20.0	19.0	19.0
Physical Gate Length for HP Logic (nm)	20	18	16	14	12	12	12
Gate LER (nm) [C]	0.8	0.7	0.6	0.5	0.4	0.4	0.4
Gate CD control (3 sigma) (nm) [B]	1.1	1.0	0.9	0.7	0.6	0.6	0.6
Overlay (3 sigma) (nm) [A]	3.6	3.0	2.4	2.0	1.6	1.6	1.6
MPU/ASIC finFET fin minimum 1/2 pitch (nm)	16.0	14.0	12.0				
FinFET Fin width (nm)	8.0	7.0	6.0				
Fin CD control (3 sigma) (nm) [B]	0.80	0.70	0.60				
FIN LER (nm) [C]	0.80	0.49	0.42				
Lateral Gate All Around (LGAA) 1/2 pitch				11	10	10	10
LGAA minimum width				7	6	6	6
LGAA CD control (3 sigma) (nm) [B]				0.7	0.6	0.6	0.6
GAA LER (nm) [C]				0.49	0.42	0.42	0.42
MPU/ASIC minimum contact hole or via pitch (nm)	51	42	34	28	23	23	23
Via CD after etch (nm) [H]	18	15	12	10.0	8.0	8.0	8.0
Contact CD (nm)after etch - finFET, LGAA	18	16	17	18	20	18	18
Chip size (mm^2)							
Maximum exposure field width (mm) [E]	26	26	26	26	26	26	26
Maximum exposure field length, i.e. scanning direction (mm) [E]	33	33	33	16.5	16.5	16.5	16.5
Maximum field area printed by exposure tool (mm^2) [E]	858	858	858	429	429	429	429
Calculated values for figures							
minimum half pitch (DRAM, MPU metal) (nm)	18	15	12	10	8	8	8
minimum half pitch (Flash, MPU fin, LGAA) (nm)	15	14	12	11	10	10	10
minimum hole pitch (DRAM, MPU, VGAA) (nm)	51	42	34	28	23	23	23
minimum contact CD after etch (DRAM, MPU, Flash) (nm)	18	15	12	10	8	8	8
minimum CD control(DRAM, MPU, Flash) (3 sigma) (nm)	1.1	1.0	0.9	0.7	0.6	0.6	0.6
minimum required OL (DRAM, Flash, MPU) 3 sigma (nm)	3.6	3.0	2.4	2.0	1.6	1.6	1.5
Estimated Cut pitch (1.4 x minimum metal pitch)	51	42	34	28	23	23	22
minimum LER (nm)	0.8	0.5	0.4	0.5	0.4	0.4	0.4
Gate Pitch	54	48	45	42	40	40	40
One half gate pitch	27	24	23	21	20	20	20
Gate lentgh (nm)	20	18	16	14	12	12	12

Fig. 2 Projected lithographic requirements for logic and DRAM. Cells that are white indicated that manufacturable solutions exist to meet this requirement and are being optimized, cells that are yellow indicate that manufacturable solutions are known that could be implemented and cells that are red indicate that manufacturable solutions are not known.

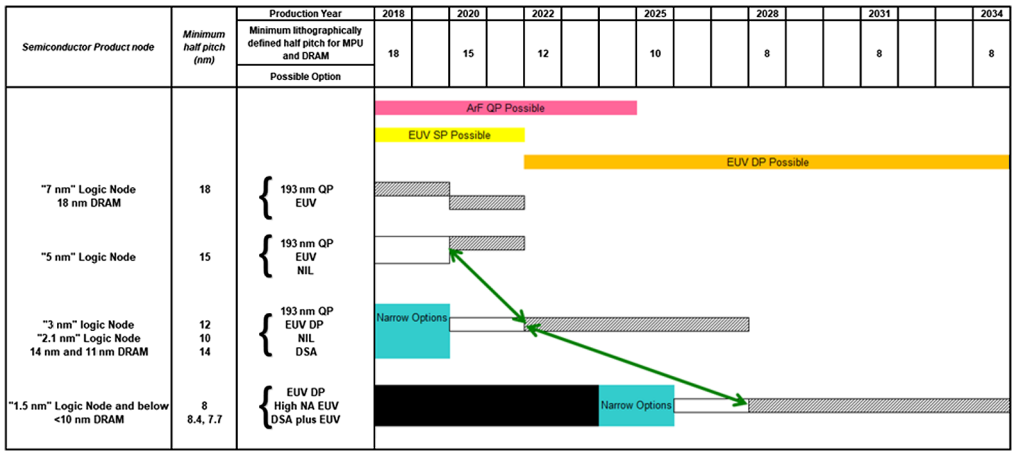

Fig. 3 Line and space potential solutions.

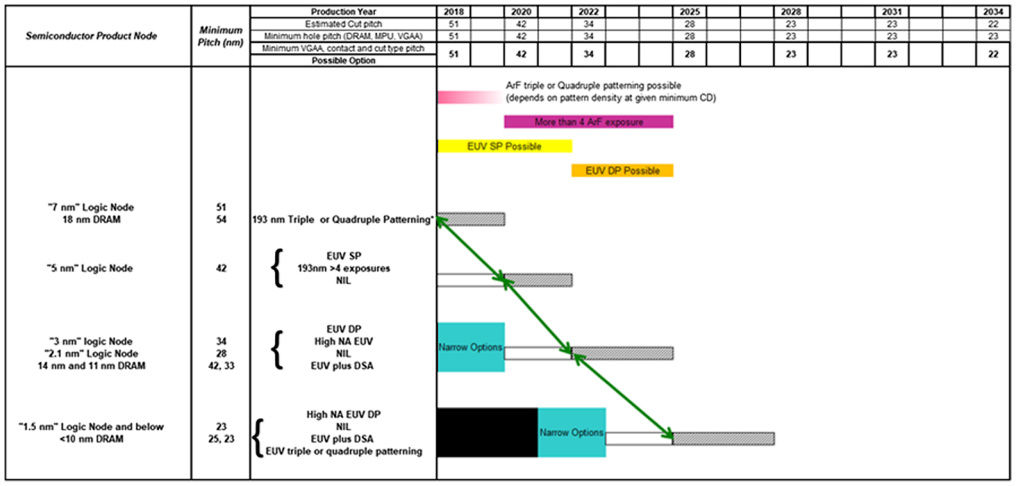

Fig. 4 Contact hole potential solutions.

expected to be in production. The white bars indicate the period when a patterning option has been selected and is being implemented but is not yet in production. During the time period right before such an implementation, a chip producer has to do work to select the patterning option that will be used from a limited set of possibilities. This is labeled as "narrow options."

For lines and spaces, EUV double patterning can provide enough resolution for any projected future critical dimension, but may not end up being the preferred solution. For contact holes and other hole type patterns, EUV double patterning at NA = 0.33 may not provide enough resolution and new solutions may be needed. Higher NA with EUV double patterning is a potential solution here.

4 Stochastics

Stochastics refers to random variations in the components of the imaging process and can be thought of as noise. Noise in imaging has multiple sources. The major ones are random variations in the aerial image due to photon shot noise and chemical variation due to randomness in the numbers and positions of the chemical components that make up resist. In EUV, there is also noise in the generation and propagation of secondary electrons, which drive the radiation chemistry in EUV resists. These noise factors affect pattern quality by influencing line edge roughness (LER), line width roughness (LWR), and critical dimension uniformity (CDU). In EUV, noise also contributes to certain sorts of defects, such as missing contacts and line opens and bridges. LER, LWR, and CDU requirements scale with resolution, so that as dimensions get smaller, these requirements get tighter. Stochastic variations do not scale in the same way as critical dimensions do, so their significance increases as critical dimensions decrease in size. This is a conflict that the lithography community is always working to resolve. The advent of EUV has brought noise issues to the fore. Not only are there 14 times fewer photons for a given exposure energy (as measured in energy per unit area), but also printed features sizes are roughly two or more times smaller than for ArF immersion, resulting in more sensitivity to all sources of noise. Noise limits the minimum feature size that can be printed with EUV.

One control factor for noise is the dose to print used for photoresist. Slower photoresists tend to show less noise than faster photoresists.[5] But EUV exposure throughput is worse with slower resist. EUV exposure tools cost well over a one hundred million dollars, so efficient usage and fast throughput for these tools is important. If the need for low noise imaging in the future forces the use of slow EUV resists, this could affect the semiconductor industry's progress along the projected IRDS roadmap. For the 2020 IRDS roadmap, the lithography team did scaling calculations to project expected dose to print as a function of critical dimension.

Our proxy for noise issues was the expected CDU for contact hole printing. Any variation in photon statistics, electron statistics, or chemical variation for small contact holes should directly

translate into a CD variation. The starting point for our calculations was the logic "7 nm" node. This node is in volume production using EUV for some critical levels. We assumed that fabs producing this node used the fastest EUV resist possible that still gave acceptable defect and noise levels. The roadmap shows the minimum contact hole dimension and the minimum target CDU that will be needed for each node. We used a CDU specification for contact holes of 15% of their printed CD. This gives an expected three sigma variation for 7 nm contact hole dimension of 3.82 nm. Smaller CDUs will require proportionally smaller CDU. This will force the use of a slower resist, all other things being equal. By calculating how much the resist photo-speed will have to change to provide this lower CDU, we can project future photo-speeds that will be needed, assuming a similar single exposure resist process is used to print all the CDs in question.

One can consider the CD variation as coming from two sources: the shot noise in the photons in the exposure and from the variation in all chemical- and electron-related processes occurring in the photoresist. The shot noise will scale as the square root of the dose to print. If all the CDU variation came from just this factor, then dose to print would have to double every time the target CD shrunk 30% for the contact hole CD variation to be the same fraction of the new node as it was of the old node. On the other hand, if all CDU was due to random resist processes, then the resist would have to improve 20% to 30% each node to reduce CDU to target levels. Neither of these limiting cases is realistic and it is known that resist feature size variation comes from both sources. It would be nice to separate the contribution from each source of variation, project the improvements of each source of variation separately, and combine the individual sources of variation separately to project overall photo-speed changes. However, we were unable to find a satisfactory breakdown of noise sources suitable for this task,[6–8] so we used a different methodology.

The k_4 equation for projecting local critical dimension uniformity (LCDU) was introduced in 2019 by Geh.[9] It calculates LCDU as a function of the quality of the aerial image as measured by the normalized image log slope (NILS), the dose to print, the energy of the photons used for imaging, and a dimensionless factor, k_4:

$$\frac{\text{LCDU}}{\text{nm}} = k_4 * \frac{1}{\text{NILS}} * \sqrt{\frac{h\nu/\text{eV}}{\text{Dose}/(\text{mJ}/\text{cm}^2)}}$$

The k_4 factor measures the quality of the process and the photoresist used to image the contact holes in the same way that the Rayleigh k_1 factor characterizes the resolution of a given resist and process.[10] The photon energy is set by the wavelength used for process in question, so for our purposes it is a constant since EUV lithography is assumed for all exposures. The NILS is affected by exposure tool factors, such as NA, aberrations, and flare, the illumination conditions used, the feature size, and by mask effects. We chose to project that NILS would be roughly constant from node to node at a value of 2.5. This is equivalent to assuming that exposure tool, reticle, process, and design improvements will occur at a rate sufficient to compensate for the loss in NILS due to smaller feature sizes and implies substantial improvement in imaging from node to node.

As described later, we used these assumptions to project future dose to print for EUV resists used to print critical dimensions. We presented this work in 2020 at the SPIE Microlithography Conference.[11] At that same conference, a revision to the k_4 formula was described.[12] In the revised formula, there is a new term $\left[e^{\left(\frac{\sqrt{2}\pi\sigma}{p}\right)^2}\right]$ added as shown in the below equation that incorporates resist blur (σ) and the pitch (p) of the feature being measured for LWR. This new term adjusts for variations in the k_4 of a resist that were observed to be a function of pattern pitch:

$$\text{LWR}_{3\sigma,unb} = k_4 * e^{\left(\frac{\sqrt{2}\pi\sigma}{p}\right)^2} * \sqrt{\frac{h\nu}{D_{\text{thr}}}} * \frac{1}{ILS}$$

This new factor, blur pitch, is necessary because resist blur affects the effective NILS of the image in the resist. In the original k_4 equation, the same resist printed at different pitches will

give different k_4 values. With the revised equation, k_4 is constant through pitch. However, in our projection of EUV dose to print, it is implicit that a different resist will be used for each node and for each critical dimension and also implicit that resist will be optimized for the particular dimension being printed. As the critical dimension shrinks, so will the optimum resist blur. The optimum resist blur for reaction diffusion is reported as 35% of the half pitch CD.[13] This means that optimized resists for each CD will have a constant ratio of σ to p. Reducing blur proportionally is not trivial. Factors such as secondary electron blur have to be addressed along with traditional factors such as acid diffusion. Historically, resist developers have reduced blur as needed, and we assumed they will continue to do this, but this is not a given. Thus, the blur pitch factor in the equation earlier will be a constant. The original k_4 equation thus shows appropriate scaling for extrapolating dose to print assuming resist blur is optimized for each successive critical dimension. Note that this methodology assumes that loss of CD control due to stochastic effects is the limiting factor in choosing resists. But stochastic effects also can create unwanted defects such as missing or merged contact holes. It has been reported that defects of this sort are more common than simply extrapolating a CD distribution using its mean and standard deviation would predict.[14–16] Understanding this sort of defect formation's effect on photo-speed and yield is something that will be worked on for the next roadmap.

To estimate how fast k_4 will improve, we turned to historical data for resist improvement. In 2002, Dammel[17] reviewed historical resist resolution improvements and translated those improvements into equivalent k_1 improvements. He found a consistent yearly improvement in resolution and a rate of improvement that was similar for both I line and KrF resists. This resolution improvement per year translates into a 6% improvement per logic node, assuming 2-year apart logic nodes.

Given a prediction for resist improvement, our prediction for constant NILS, and the roadmap's requirements for LCDU, we can then calculate the photo speed that will make the k_4 equation work. Inserting values for NILS, k_4, and the 7 nm node LCDU target into the formula for k_4 gives a nominal dose to print of 36 mJ/cm^2 for 7 nm critical dimension contact holes. Using a 6% improvement in k_4 for each successive future node and using the targeted LCDU gives a projected dose to print for each future node. The projected doses to print for each logic node are shown in Fig. 5 along with the percentage increase in dose to print each node compared to the previous node. The results are shown graphically in Fig. 6. Note that the projected doses to print start dropping in 2031 because logic switches to 3D scaling and critical dimensions no longer shrink, but resist is projected to continue to improve.

The dose to print is projected to rise to over 100 mJ/cm^2 in 2028. This prediction is in line with recent stochastic simulations of EUV resist chemistries.[18] These simulations included

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
	G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.5"	"1.5"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i2.1-f1.5	i2.1-f1.5
Calculated Resist Dose to meet target LCDU (mJ/cm2)	36	46	64	81	112	99	95
Node to node percent change in dose		27%	38%	27%	38%	-12%	-5%

Fig. 5 EUV dose to print roadmap.

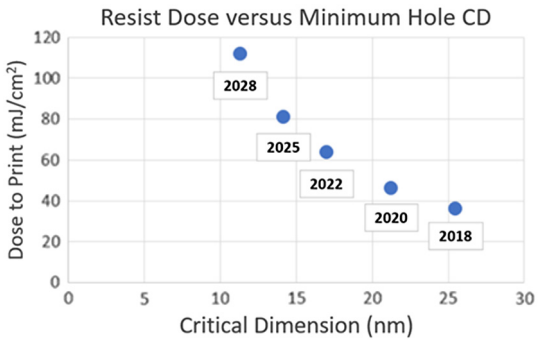

Fig. 6 EUV dose to print versus critical dimension.

electron blur, and they predicted that no combination of resist composition factors will result in a resist that images 10 nm lines and spaces without unacceptable defect levels unless the dose to print is over 100 mJ/cm^2. The match of our macroscale k_4-based prediction with this literature prediction based on detailed physics gives confidence that a 6% improvement per node was realistic.

A sensitivity analysis shows that if the starting k_4 value or starting NILS values assumed for the 7 nm logic node are varied, then the dose to print for 7 nm node patterns will vary, but the percentage increases in dose to print from node to node will be the same. However, the rate of increase in dose to print is sensitive to the improvement in resist as measured by k_4. Figure 7 shows the expected dose to print as a function of node for different rates of improvement in k_4.

If resist stochastics do not improve with resist optimization, then resist dose to print will increase fivefold over 5 nodes. If resist stochastics improve so much that k_4 improves 15% every node, the dose to print increases less than 50% over the same five nodes. Given this large dependance on the rate of resist stochastic improvement, it is useful to consider the factors that might make improvement slower or faster than the published roadmap's estimate of 6% improvement per node.

In published studies of EUV resist improvement, some have shown very little improvement from year to year. (Reference 19 shows new resist falling on the same LER photospeed curve as old resists.) New resists have fallen along the existing trade-off between dose to print and line roughness. But some recent papers have shown quite spectacular improvements in resists for particular applications or particular imaging conditions.[20] Part of this dichotomy may be because there two classes of EUV resists in current use. There are chemically amplified resists that use mostly or all organic chemistry and there are mostly inorganic resists that use metal oxides as the key EUV imaging component. Chemically amplified systems operate by principles that were well established when they were applied to KrF and ArF imaging. It is hard to expect rapid improvement in resists based on well-established mechanisms that have already been optimized for stochastics in ArF applications. And some might argue that the source of noise is well understood and there is a lower limit to the LWR, LER, or CDU one can achieve.[21] The inorganic resists are a new class of resists not used for previous wavelengths, so one might expect they will improve faster than EUV chemically amplified resists will. The metal-based resists for EUV have already matched conventional chemically amplified resist in performance.[22] However, the inorganic resists are only available in negative tone, giving an advantage to organic-based chemically amplified resists in certain applications.

The methodology described here is high level and does not look at details of how to do the actual improvements we project. For example, it does not look at specific issues in resist such as electron blur or competing EUV caused reactions. It does not consider alternative processes, such as DSA repair of defects that may enable low EUV dose to prints. It is an extrapolation

YEAR OF PRODUCTION	***2018***	***2020***	***2022***	***2025***	***2028***
	G54M36	**G48M30**	**G45M24**	**G42M21**	**G40M16**
Logic industry "Node Range" Labeling (nm)	**"7"**	**"5"**	**"3"**	**"2.1"**	**"1.5"**
IDM-Foundry node labeling	**i10-f7**	**i7-f5**	**i5-f3**	**i3-f2.1**	**i2.1-f1.5**
Mainstream device for logic	**finFET**	**finFET**	**finFET**	**LGAA**	**LGAA**
EUV Single Patterning					
minimum hole pitch (via, contact, cut)	**51**	**42**	**34**	**28**	**23**
Minimum hole CD size on mask (wafer scale) [2]	**31**	**25**	**20**	**17**	**14**
Printed Contact Hole CD	**25**	**21**	**17**	**14**	**11**
Contact Hole LCDU requirement (15% of printed CD) (nm) [3]	**3.82**	**3.18**	**2.55**	**2.12**	**1.70**
Photospeed Extrapolation in mJ/cm^2					
No Improvements in k $_4$	**36**	**52**	**82**	**118**	**184**
k $_4$ improves 6% per node	**36**	**46**	**64**	**81**	**112**
k $_4$ improves 10% per node	**36**	**42**	**54**	**63**	**79**
k $_4$ improves 15% per node	**36**	**38**	**43**	**44**	**50**

Fig. 7 Increase in dose to print for different rates of k_4 improvement.

based on our understanding of how technology has improved in the past. It shows what challenges there are but does not give a solution for solving them. Historically, the industry has met difficult challenges in the past with both innovation and incremental improvements. The entire lithographic committee hopes this continues to happen in the future.

The IRDS considers that 6% improvements in k_4 would also represent a substantial rate of resist improvement. But, in the end, this 6% value is a prediction of the future by a committee of experts, not an experimentally determined number. Research in experimental psychology is not kind to such predictions,[23] at least in the field of politics. The author of this article makes the following suggestion. Any interested reader of this article can send their own prediction of the improvement in k_4 for each logic node to the corresponding author's email address. If there are enough responses, the results will be included in the next available edition of the IRDS lithography roadmap.

The projected rise in dose to print would impose large costs on EUV users due to reduction in throughput and/or increases in exposure tool costs. One alternative is the use of EUV double exposure. This will increase litho costs but provide improved stochastics due to the larger printed dimensions in photoresist. Research is already underway comparing single exposure to double exposure for EUV applications.[24,25] Another strategy is to accept bad stochastics but find process alternatives that improve pattern quality. Double patterning is one such process.[26] Directed self-assembly also shows potential for enabling use of much faster resists. (A paper was presented at the SPIE Microlithography Conference of 2020, "Enabling Moore's law with DSA," by G. Singh, E. Han, and F. Gstrein. Unfortunately, no proceedings paper is available. A follow-on paper was presented in 2021 by Ref. 27). Process improvements can also help. An example of a process improvement is printing larger vias than needed to get less CDU and then shrinking them afterward by etch or some other process. New resist types and processes could also arise. Work has recently been reported on dry deposited and developed resists,[28] but there is not enough published data to compare their stochastics to current materials.

5 Challenges

There are other challenges besides noise-related pattern quality. Edge placement error (EPE) is a leading challenge for future nodes. Requirements for EPE are functions of the final feature size, and EPE requirements shrink as CDs get smaller. Processes that relax printed CD requirements, such as double patterning, often make EPE worse. Maintaining acceptable NILS as printed feature size decreases will require improvements in masks, exposure tools, and source mask optimization along with possible chip design changes to enable easier imaging. Higher NA EUV exposure tools with an NA of 0.55 are projected to be available in 2023 or 2024. These higher NA tools will improve NILS for a particular feature size compared to lower NA imaging. These tools will have half the exposure field size of current tools and may require field stitching for some product designs. They will require improved reticles. The higher illumination and imaging angles in the exposure tool may reduce depth of focus due to focus sensitive EPE and also reduce image contrast. Solutions to these challenges are not yet demonstrated.

The industry is actively investigating alternative printing techniques, such as nanoimprint, directed self-assembly, and direct write. Nanoimprint has shown substantial recent progress[29] but still has not shown sufficient productivity for use in volume memory chip production or sufficiently low levels of defects to be considered for leading edge logic use. It also needs improvements in overlay to be used for logic. Directed self-assembly still has not been demonstrated in volume production. Direct write does not have sufficient throughput for high-volume chip productions but has advantages for low-volume production where leading-edge dimensions are not required. Recent papers have described new direct write tools under development.[30,31]

For the long term, when logic starts scaling vertically instead of by shrinking critical dimensions, yield and process complexity will be critical challenges. The roadmap predicts three-dimensional logic will be in production in 2031, but addressing its challenges and developing such devices will have to start much sooner than that. The 2021 Lithography Difficult Challenges are shown in Fig. 8.

Next Generation Technology	First Possible Use in HVM	Feature Type	Device Type	Key Challenges	Required Date for Decision making
EUV Multiple Patterning	2022	12 nm hp LS	"3 nm" Logic Node	• Process control (EPE, overlay, CDU, LER/LWR) • Cost/throughput	2021
EUV high NA	2025	10.5 nm hp LS	"2.1 nm" Logic Node	• Resist capability (sensitivity, LER/LWR, resolution , defects) • Stitching of two mask patterns • Improved masks for high NA • Cost/Throughput	2024
NanoImprint	2021	20 nm lines and spaces 20 to 30 nm contact holes	3D Flash Memory	• Defectivity • Overlay • Master Template fabrication and inspection <20 nm • Defect repair • Mass-production capacity	Product Evaluation Underway
DSA (for pitch multiplication)	2022	Contact holes/cut levels for logic Possibly nanowire patterning	"3 nm" Logic Node	• Defectivity and defect inspection • Pattern Placement • Design • 3D Metrology	2021

Fig. 8 IRDS 2021 lithography difficult challenges.

6 Conclusions

The IRDS roadmap projects future challenges for semiconductors and possible solutions to those challenges. It shows that logic devices will drive shrinking critical dimensions and improvements in patterning for roughly the next 10 years. After that, logic will switch to vertical scaling. The lithography section of the IRDS roadmap addresses these patterning challenges. It includes projected patterning requirements and possible patterning options. A major challenge is noise in imaging. Requirements for low defects and good pattern quality will drive increases in EUV dose to print as printed features get smaller. Even assuming substantial improvements in resists, tools, and other imaging infrastructure, a dose to print of over 100 $\mathrm{mJ/cm^2}$ is projected in 2028 if alternative processes or designs are not implemented that mitigate noise effects. This estimate is sensitive to the rate of improvement projected for resist stochastics. Even assuming that

Member Name	Organization	Region		Member Name	Organization	Region
Hajime Aoyama	Nikon	Japan		Ted Fedynyshyn	MIT Lincoln Laboratory	USA
Heiko Feldmann	Zeiss	Europe		David Fried	Lam Research	USA
Reiner Garreis	Zeiss	Europe		Naoya Hayashi	Dai Nippon Printing	Japan
Craig Higgins	KLA	USA		Erik Hosler	PsiQuantum LLC	USA
Hidemi Ishiuchi	Kioxia	Japan		Insung Kim	Samsung	Korea
Ryoung-han Kim	IMEC	Europe		Seomin Kim	SK Hynix	Korea
David Kyser	Semiconductor Industry Consultant	USA		Michael Lercel	ASML	USA
Harry Levinson	HJL Lithography	USA		Isao Mita	Sony Semiconductor Solutions	Japan
Tsuyoshi Nakamura	TOK	Japan		Mark Neisser	Tan Kah Kee Innovation Lab	China
Shinji Okazaki	Alitecs	Japan		Laurent Pain	LETI	Europe
Doug Resnick	Canon Nanotechnologies	USA		Tadatake Sato	AIST	Japan
Kiwamu Sue	AIST	Japan		Raluca Tiron	LETI	Europe
Walt Trybula	Trybula Foundation, Inc.	USA		Takeo Watanabe	Un. of Hyogo	Japan
John Wiesner	IC Lithography Consultant	USA		Jim Wiley	IC Lithography Consultant	USA
Stefan Wurm	ATICE, LLC	USA		Shusuke Yoshitake	NuFlare Technology	Japan

Fig. 9 Current IRDS lithography team membership.

stochastics are controlled well enough to give sufficient LWR and CDU, other factors such as missing or merged features, or inability of resist to function reliably at reduced dimensions, may be a roadblock to future EUV use. Other major challenges are improved EPE, and the development and implementation of high NA EUV imaging. The industry is actively pursuing alternative patterning technologies, particularly nanoimprint lithography, directed self-assemble, and direct write. For the long term, as semiconductor scaling changes to 3D scaling, particular patterning challenges will be yield and process complexity.

Acknowledgments

The lithography roadmap is the product of an entire team of people and all their contributions are gratefully acknowledged. Without their work, the roadmap would not be possible. The current membership is shown in Fig. 9.

References

1. G. Moore, "The future of integrated electronics," Fairchild Semiconductor Internal Publication (1964).
2. G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff.," *IEEE Solid-State Circuits Soc. Newsletter* **11**(3), 33–35 (2006).
3. https://irds.ieee.org/
4. J. Van Schoot et al., "High-NA EUV lithography exposure tool: key advantages and program progress," *Proc. SPIE* **11609**, 1160905 (2021).
5. M. Neisser et al., "Novel resist approaches to enable EUV lithography in high volume manufacturing and extensions to future nodes," *Proc. SPIE* **9422**, 94220L (2015).
6. P. Naulleau and G. Gallatin, "Relative importance of various stochastic terms and EUV patterning," *J. Micro/Nanolithogr. MEMS MOEMS* **17**(4), 041015 (2018).
7. A. Chunder et al., "Separating the optical contributions to line-edge roughness in EUV lithography using stochastic simulations," *Proc. SPIE* **10146**, 101460B (2017).
8. M. Neisser et al., "EUV research activity at SEMATECH," *J. Photopolym. Sci. Technol.* **27**(5), 595 (2014).
9. B. Geh, "EUVL: the natural evolution of optical microlithography," *Proc. SPIE* **10957**, 1095705 (2019).
10. http://www.lithoguru.com/scientist/CHE323/Lecture48.pdf
11. M. Neisser and H. J. Levinson, "Projecting EUV photo-speeds for future logic nodes," *Proc. SPIE* **11323**, 113231N (2020).
12. J. G. Santaclara et al., "One metric to rule them all: new k_4 definition for photoresist characterization," *Proc. SPIE* **11323**, 113231A (2020).
13. C. A. Mack, "Reducing roughness in extreme ultraviolet lithography," *J. Micro/Nanolithogr. MEMS MOEMS* **17**(4), 041006 (2018).
14. T. A. Brunner et al., "Line-edge roughness performance targets for EUV lithography," *Proc. SPIE* **10143**, 101430E (2017).
15. R. L. Bristol and M. E. Krysak, "Lithographic stochastics: beyond 3σ," *J. Micro/Nanolithogr. MEMS MOEMS* **16**(2) 023505 (2017).
16. A. R. Neureuther, L. Long, and P. Naulleau, "Modeling stochastic effects of exposure/diffusion and dissolution on missing contacts," *Proc. SPIE* **11609**, 1160914 (2021).
17. R. R. Dammel, "Photoresists for microlithography, or the Red Queen's race," *J. Micro/Nanolithogr. MEMS MOEMS* **1**(3), 270–271 (2002).
18. H. Fukuda, "Impact of asymmetrically localized and cascading secondary electron generation on stochastic defects in EUV lithography," *Proc. SPIE* **10957**, 109570G (2019).
19. A.-M. Goethals et al., "Progress on EUV resist materials and processes at IMEC," in *Int. EUVL Symp.*, Washington DC (2014).
20. T. Allenet et al., "Progress in EUV-interference lithography resist screening towards the deployment of high-NA lithography," *Proc. SPIE* **11609**, 116090J (2021).

21. J. J. Biafore and M. D. Smith, "Application of stochastic modeling to resist optimization problems," *Proc. SPIE* **8325**, 83250H (2012).
22. X. Wang et al., "Progress in EUV resists towards high-NA EUV lithography," *Proc. SPIE* **10957**, 109570A (2019).
23. P. E. Tetlock, *Expert Political Judgment: How Good Is It? How Can We Know?* Princeton University Press, New Jersey (2005).
24. D. De Simone et al., "28 nm pitch single exposure patterning readiness by metal oxide resist on 0.33NA EUV lithography," *Proc. SPIE* **11609**, 116090Q (2021).
25. A. Dutta et al., "Strategies for aggressive scaling of EUV multi-patterning to sub-20 nm features," *Proc. SPIE* **11323**, 113230V (2020).
26. D. B. Millward et al., "Graphoepitaxial and chemoepitaxial methods for creating line-space patterns at 33nm pitch: comparison to a HVM process," *Proc. SPIE* **9423**, 942304 (2015).
27. F. Gstrein, "Scaling opportunities with next-generation, multi-pitch directed self assembly," *Proc. SPIE* **11610**, 116100J (2021).
28. M. Alvi et al., "Lithographic performance of the first entirely dry process for EUV lithography," https://euvlitho.com/2020/2020%20EUVL%20Workshop%20Keynote%20Weidman.pdf
29. A. Kimura et al., "Nanoimprint system alignment and overlay improvement for high volume semiconductor manufacturing," *Proc. SPIE* **11324**, 113240B (2020).
30. D. G. Flagello, "Recent developments and concepts in optical exposure technology," *Proc. SPIE* **11613**, 1161304 (2021).
31. D. K. Lam, "Multicolumn e-beam lithography (MEBL) for IC traceability: MEBL enables chip ID to thwart tampering/counterfeiting," *Proc. SPIE* **11324**, 113240P (2020).

Mark Neisser is the technology director for the Industrialization Platform at the Tan Kah Kee Innovation Laboratory in Xiamen, China. He is also an adjunct professor in the School of Electronic Science and Engineering at Xiamen University. He received his BS degree in chemistry from Cornell University and his MS and PhD degrees from the University of Michigan. He is the author of more than 30 patents, over 100 journal papers, and has co-authored two book chapters. He is the chairman of the IRDS Roadmap Lithography Committee. He is a member of SPIE.