Journal of Photonics for Energy

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Rakeshkumar V. Mahto, Deepak K. Sharma, Dinosha X. Xavier, Raksha N. Raghavan, "Improving performance of photovoltaic panel by reconfigurability in partial shading condition," *J. Photon. Energy* **10**(4), 042004 (2020), doi: 10.1117/1.JPE.10.042004

Improving performance of photovoltaic panel by reconfigurability in partial shading condition

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Abstract. A photovoltaic (PV) panel operating in partial shading condition results in lowering its power efficiency. In a worst-case scenario, it can create a hotspot that can eventually cause a fire hazard. To address this issue, bypass diodes are connected across a group of PV cells having series-parallel (SP) configuration. Owing to the placement bypass diodes in the PV panel, it can circumvent unshaded PV cells. Hence, topologies such as total cross-tied (TCT), bridge link (BL), and honeycomb (HC) for PV panels are proposed besides SP to reduce the effect of partial shading. Each configuration demonstrated advantages over SP topology. However, many of these configurations lack a mechanism to isolate PV cells that are affected due to the hotspot. Recently developed complementary metal oxide semiconductor (CMOS)-embedded PV panel has been shown to offer many other benefits besides effectively dealing with shading conditions. We are comparing the performance of CMOS-embedded PV panel under various partial shading conditions with PV panel with fixed configuration topologies, such as SP, TCT, BL, and HC. SPICE-based equivalent PV modeling technique is used in this research to compare the maximum power generated in different topologies under changing partial shading conditions. Results show that CMOS-embedded PV panels are more efficient in coping with partial shading conditions compared to any other contemporary fixed topologies. [DOI: 10.1117/1.JPE.10.042004]

Keywords: photovoltaics; CMOS; partial shading; hotspot; reconfigurability; embedded systems; efficiency.

Paper 19094SS received Nov. 1, 2019; accepted for publication Jan. 30, 2020; published online Feb. 14, 2020.

1 Introduction

Power is an undisputed lifeline in today's high-tech world. Mass awareness drives have created significant cognizance toward sustainable and green technologies in the past quarter-century in response to the depletion of fossil fuels and volatility of energy prices. Photovoltaics (PV)-based, sustainable, and green-technology-based power sources are in high demand due to their ability to meet industrial, commercial, and residential demands. Government incentives available to consumers for PV-based renewable energy systems have further fueled their acceptance. Due to the consistently increasing popularity of PV-based energy, many advancements have happened that enable improving its performance and reducing its cost. Recent advancements in silicon processing have increased the efficiency of single-crystalline silicon-based PV cells by 28%.[1] Also, many advanced maximum power point tracking algorithms are now available that enable harvesting higher amounts of energy from a PV panel.[2] Despite these improvements in solar energy harvesting, PV modules still use series-parallel (SP)-based fixed topology. As a result, a PV module remains vulnerable to such issues as partial shading,[3,4] irradiance fluctuation,[5–8] mismatch,[9–11] and faulty conditions,[12–15] which are known to severely affect its power

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Table 1 Comparison between the performances of fixed topology PV module in different shading conditions.

Reference	Series-parallel	Total cross-tied	Bridge link	Honeycomb
18, 23, and 27	✓	✓	✓	✓
19, 20, and 28	✓	✓		
21, 22, 24, 25, and 30	✓	✓	✓	
31	✓			✓

efficiency and performance. In response, most of the PV modules are equipped with a bypass diode to minimize the effects of such issues.[15–17]

Besides the typical SP topology, topologies such as total cross-tied (TCT),[18–20] bridge link (BL),[21] and honeycomb (HC)[22] are being considered and analyzed in different partial shading conditions.[22–31] Performance of each topology varies under different shading patterns, and their performance has proven to be better than the regular SP topology. However, each topology has advantages and disadvantages under different conditions.[18–31]

A PV module embedded with complementary metal oxide semiconductor (CMOS) switches has recently been proposed as an alternative to the SP-based PV module with bypass diode.[32–39] Studies have shown that PV modules embedded with switches have better capability for dealing with partial shading, mismatch issues, and faulty conditions.[32,33,35,37] Additionally, such PV modules reconfigure in real-time (i.e., an number of PV cells connected in series × number of cells connected in parallel change), which enables creating a power island.[36] Among all switches, CMOS-based switches are ideal for creating a reconfigurable PV module, since they can be easily integrated with PV cells in a single die, i.e., monolithic CMOS-on-PV.[36,39] However, unlike all other contemporary topologies, the reconfigurable PV module requires a controller, a computing device, and an algorithm for partial shading or fault detection. Therefore, a comparative study between the reconfigurable PV modules with these newer topologies is required to better understand the effectiveness of switches in alleviating the limitations in the PV module.

In this paper, we are presenting a comparative analysis between reconfigurable PV modules and traditional PV configurations, namely SP, TCT, BL, and HC, operating under different shading patterns. Such a comparison between fixed topologies and reconfigurable PV modules has not been done in any previous studies. Only fixed topologies are compared among themselves in different partial shading conditions, as shown in Table 1. This research effort is vital to weigh-in, adding complexity in a PV module for improving the performance during partial shading conditions. In addition, through this paper, we build upon the previous research conducted in this area[40] and add to the existing body of knowledge by including a bypass diode in our study, which was not included in previous studies. Having a bypass diode in PV systems is an industry norm, and hence this analysis will help in understanding how each configuration responds to various partial shading conditions. This research determines the best alternative to SP topology-based PV module with bypass diode, to create a futuristic smarter PV module. Simulation and performance analysis of the PV array is done using SPICE,[41] which was used to evaluate the performance of SP, TCT, BL, and HC in Refs. 23–28 and 31. It is envisioned that this research will lay the foundation for future research and help the PV industry excel.

2 Preliminary

2.1 *Different Topologies in PV Modules*

In this section, SP, BL, HC, and CMOS-embedded PV configurations are presented to explain the difference in their internal connections. We also discussed the SPICE-based PV modeling technique as it is used for comparison in this research.

2.1.1 *Series and parallel*

SP configuration is a traditionally used configuration, where each PV cell is connected in series to increase the voltage. These series connected PV cells are then connected in parallel to increase the current in the panel. Therefore, the output voltage of the PV module is proportional to the number of PV cells in series connection, and the output current of the PV array is proportional to the total number of parallelly connected series of PV cells. The fact that this configuration is economical, easy to build, and requires no additional components has elevated it as an industry standard.[26] However, the average efficiency of power and decreasing current under unfavorable circumstances have paved the way for inventing more efficient and cost-effective configurations. An SP topology with four series connected in parallel wherein each series consists of eight PV cells is shown in Fig. 1(a). We are assuming a bypass diode is connected across each PV cell present in the PV module, as shown in Fig. 1(a).

2.1.2 *Total cross-tied*

The TCT topology is similar to the SP configuration. Each PV cell in a row of parallelly connected PV cells is tied to the neighboring cells.[29] This ensures that voltage across the PV cells tied together remains the same. Hence, the total voltage across a PV panel in TCT topology is equal to the summation of voltage across each cross-tied PV cell in the panel. The total number of bypass diodes used in TCT topology is much less compared to SP topology owing to the cross-tied connection between PV cells. Hence, due to its simplicity, similar to the SP topology, TCT can also be used for the mass production of PV panels. A PV panel consisting of 32 PV cells that are using TCT topology is shown in Fig. 1(b).

2.1.3 *Bridge link*

BL configuration is a type of cross-tied topology that is interconnected in a bridge-rectifier way. In this configuration, two or more series of PV modules are connected in parallel with two

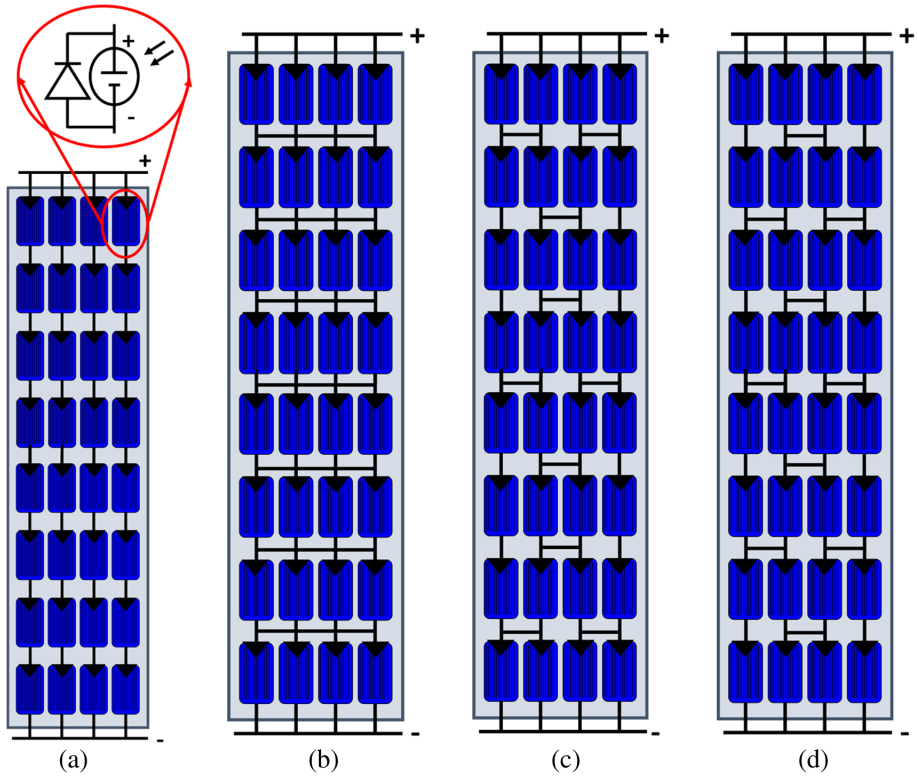

Fig. 1 Fixed configuration of PV module with 32 PV cells: (a) SP PV module integrated with bypass diode connected across each PV cell in module (b) TCT, (c) HC, and (d) BL.

parallel strings that create a tie between the series giving an appearance like a bridge.[26] The number of parallel connections between the series of PV modules is less than that of the TCT configuration but more than that of the SP configuration.

The disadvantage of BL configuration to the SP configuration is that the structure of BL configuration is complex to build, and a higher number of switching devices are required. However, these drawbacks are overlooked as the performance of BL is comparatively higher than that of the SP configuration under shaded conditions.[14,26]

2.1.4 *Honeycomb*

Just like the BL configuration, honeycomb (HC) configuration is a type of TCT configuration. It is connected in a hexagonal pattern that replicates a honeycomb structure, and hence the name "honeycomb" is used.[29] The series connections between the PV modules is comparatively less than that of the traditional SP configuration. This decrease in the series connection will help to improve the mismatching power loss that usually occurs in the PV module. The interconnection for the 32 PV cells-based PV panel using HC topology is shown in Fig. 1(d).

2.1.5 *Photovoltaics embedded with CMOS switches*

A typical reconfigurable PV module consists of three key components: reconfigurable PV module, embedded computing system, and an algorithm. The block diagram of a complete system-level reconfigurable PV module is shown in Fig. 2.

Reconfigurable PV module embedded with CMOS switches. Figure 3(a) shows a PV panel where each PV cell is embedded with CMOS-based addressable programmable switches (APS). The CMOS-based APS switches are shown in Fig. 3(b).

The total number of APS in a PV panel is one less than the total number of PV cells present in the panel. Each APS switch will have its own 6-bit digital reference address. These APS switches are connected to a common clock, data, and reset signals. The data packet that is sent serially through the data signal is of 9 bits. The least significant 6 bits consist of a digital address,

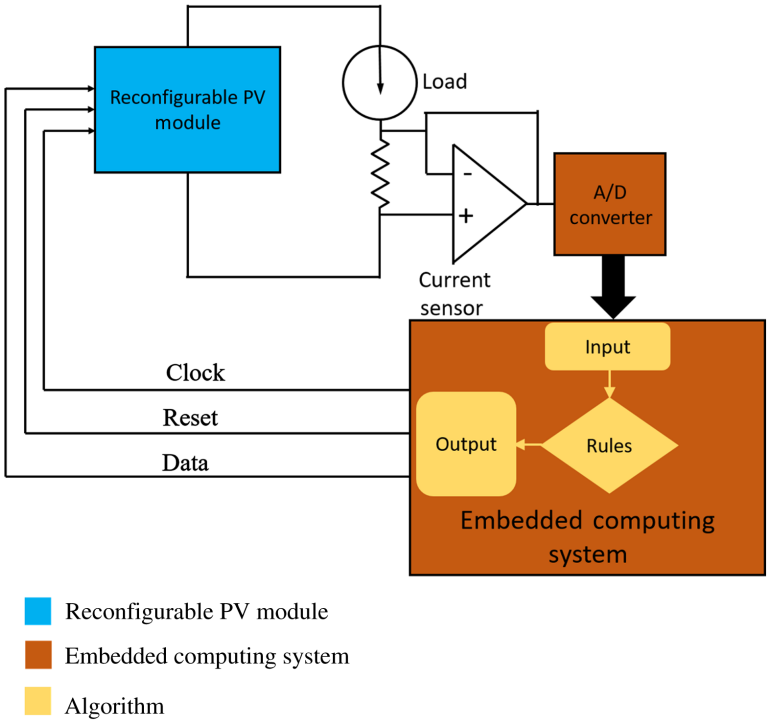

Fig. 2 Block diagram of reconfigurable PV module controlled by an embedded computing system.

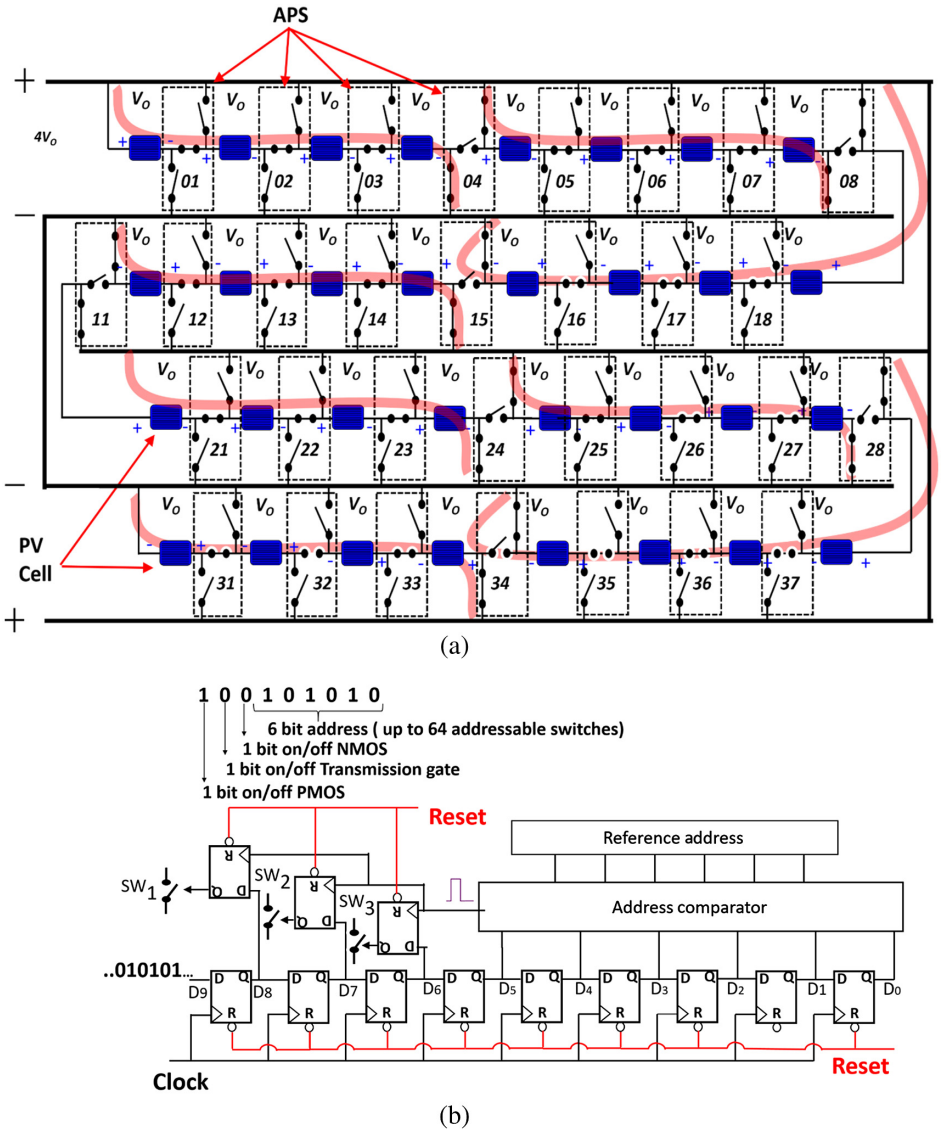

Fig. 3 (a) PV module embedded with CMOS-based APS (b) 9-bit APS.

whereas the 3 most significant bits are for turning-on or turning-off switches SW_1, SW_2, and SW_3, as shown in Fig. 3(b). The switch SW_1 enables connecting a PV cell to the negative terminal, and switch SW_3 lets the PV cell connect to the positive terminal. The switch SW_2 enables connecting two PV cells in series. Compared to the switch-embedded PV module embedded with switches presented in Refs. 32, 33, and 37, the CMOS-embedded PV module shown in Fig. 3 is three times faster.[38] The increased speed is a result of APS turning ON/OFF three switches (SW_1, SW_2, and SW_3) simultaneously compared to one serial line controlling only one switch at a time.

Consider a CMOS-embedded PV panel consists of 32 PV cells. This will require 31 APS, as shown in Fig. 3(a). Assuming the CMOS-embedded PV panel is in 4×8 configuration, representing the number of PV cells in parallel $\times$ the number of PV cells in series. Consider that the user wants to change the configuration from 4×8 to 4×7 configuration. For changing the configuration, the APS switches required to be modified are identified by the user. Later, the data packet for those APS switches is generated and sent serially through the data line. Consider that each APS switch has the address shown in Fig. 3(a). Among the several ways of changing, the configuring from 4×8 to 4×7 data packets in the following order must be sent to the PV array.

i. Initially, a 9-bit data packet of "1000100010" is sent serially to the PV array.
ii. The 3-bit most significant bit, "100", will turn off switch SW_2 and SW_3 for the APS with the digital address of "0100010."
iii. The switch SW_1 in APS with a digital reference address of "0100010" will be turned on. Since other APS have separate digital reference address; therefore, the received data packet will not affect them.

Embedded computing system. The role of the embedded computing system is to measure the output power delivered to the load, process it, and then generate appropriate output signals to change the configuration of the reconfigurable PV module. Depending on the discrepancy between the measured power and computing power, the algorithm will generate data packets to change the configuration of the reconfigurable PV module. This data packet is then sent through the serial data line to each APS switch in the reconfigurable PV module as shown in Fig. 2. Besides that, the embedded computing system will also generate and send the reset and clock signal to all APS switches present in the reconfigurable PV module. Over the years, many different kinds of embedded systems are used, such as computers,[32,33,37] field programmable gate array,[38,39] and Raspberry PI.[42]

Algorithm. The algorithm for a reconfigurable PV module is presented in Refs. 32, 33, and 37–39. The algorithms developed and implemented for the reconfigurable PV module adhere to the following steps.

i. The embedded computing system will compute the expected power generated that is presented as P_{Expected} in Fig. 4.
ii. The P_{Expected} will be compared with the measured powered, P_{Measured} recorded by the embedded computing system.
iii. If the P_{Measured} and P_{Expected} are equal, there exists no shading condition. On the contrary, if they are not equal that means shaded PV cells are present in the module as shown in Fig. 4.
iv. Once the presence of the shaded PV cells is detected then the goal of the algorithm is to detect the exact location of the shaded PV cells in the panel. Various techniques for shaded PV cell detection are presented in Refs. 32, 33, and 37–39. In Refs. 32 and 39, first row and then column is scanned one after another to identify the location of shaded PV cells.

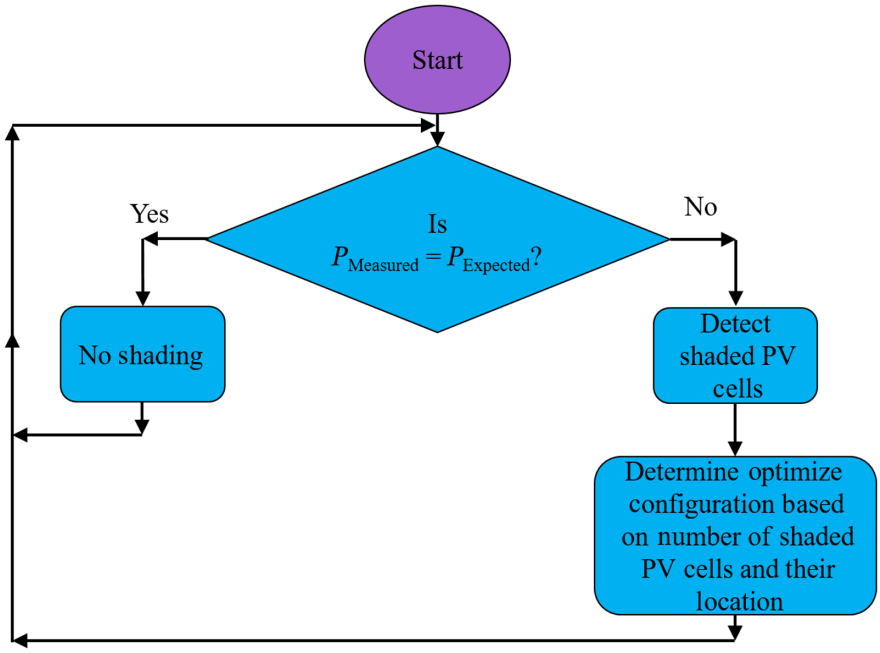

Fig. 4 Flowchart explaining the algorithm for shaded PV cells detection and mitigation.

However, this technique is tedious and time consuming. Later, a dynamic programming-based shaded PV cell detection was presented in Ref. 33. After identifying the location of the shaded PV cells, the algorithm's goal is to determine the optimal configuration of the PV module to maximizing power generation.

2.2 *Modeling of PV Cells and Module*

For modeling the PV cells, two-diode-based equivalent circuit from Ref. 41 will be used, as shown in Fig. 5. The parameter I_{ph} shown in Fig. 5 is photon current. The photon current is dependent on the area of the PV cell and solar irradiation. The photon current, I_{ph}, across a PV cell is computed by Eq. (1), where J_{SC} is the short circuit current density in A/cm^2, and A_{PV} is the area of the PV cells in cm^2. The I_{d1} and I_{d2} are the diode current across the two diodes, respectively. The diode current is computed using Eq. (3), where I_s is the saturation current of the diode (Table 2).

$$I_{ph} = J_{sc} \times A_{PV} \times \frac{G}{G_{STC}}, \tag{1}$$

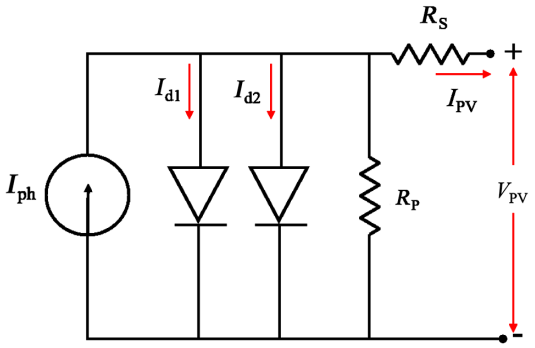

Fig. 5 Double diode-based equivalent PV cell modeling.

Table 2 Parameters for PV cell equivalent circuit model.

Symbol	Description	Value and units
V_{PV}	Output voltage across PV cell	Voltage
I_{PV}	Output current from PV cell	Amperes
V_{OV}	Open load voltage	0.55 V
I_{Ph}	Photon current	2.17 A
R_P	Internal shunt resistor	1×10^{-3} Ω
R_S	Internal series resistor	100 kΩ
A_{PV}	Area of PV cell	126.6 cm^2
J_{SC}	Short-circuit current density	34.3 mA/cm^2
V_T	Thermal voltage	26 mV
A	Diode ideality constant	
I_S	Diode saturation current	$I_{S1} = 1.27$ nA and $I_{S2} = 127$ nA
G	Solar irradiation data	1000 W/m^2
G_{SC}	Shaded solar irradiation data	500 W/m^2

$$I_{\mathrm{PV}} = I_{\mathrm{ph}} - I_{d1} - I_{d2} - \left(\frac{v_{\mathrm{PV}} + i_{\mathrm{PV}} \cdot R_S}{R_P}\right), \tag{2}$$

$$I_d = I_S \left[e^{\left(\frac{V_{\mathrm{PV}} - I_{\mathrm{PV}} \cdot R_S}{A \cdot V_t}\right)} - 1 \right]. \tag{3}$$

I_{PV} in Fig. 5 is the current generated by the PV cells that can be calculated by Eq. (2).

3 Experimental Setup

The shading pattern used for the experiment is shown in Fig. 6. For comparing the performance of each type of topology, we are considering a PV module consisting of 32 PV cells in 8×4 configuration. The PV cells arranged in each PV panel will be similar, except the topology by which they are connected with each other is different.

Also, for simplicity, all the PV cells in the PV panel are assumed to be homogeneous, with no mismatch between them. The solar irradiance of unshaded and shaded PV cells is equal to 1000 and 500 $\mathrm{W/m^2}$, respectively. The current versus voltage (I–V) and power versus voltage (P–V) characteristics of the PV module configured in various topologies (SP, TCT, BL, and HC) are simulated using PSpice. During the I–V and P–V characteristics, the PV panel is assumed to be operating at a constant temperature of 25°C. The I–V and P–V characteristics for PV panel in SP topology with 32 PV cells for no shading and the shading pattern is presented in Fig. 7. This characteristic is shown in Fig. 7, which is obtained by SPICE simulation using two-diode-based equivalent circuit.[41]

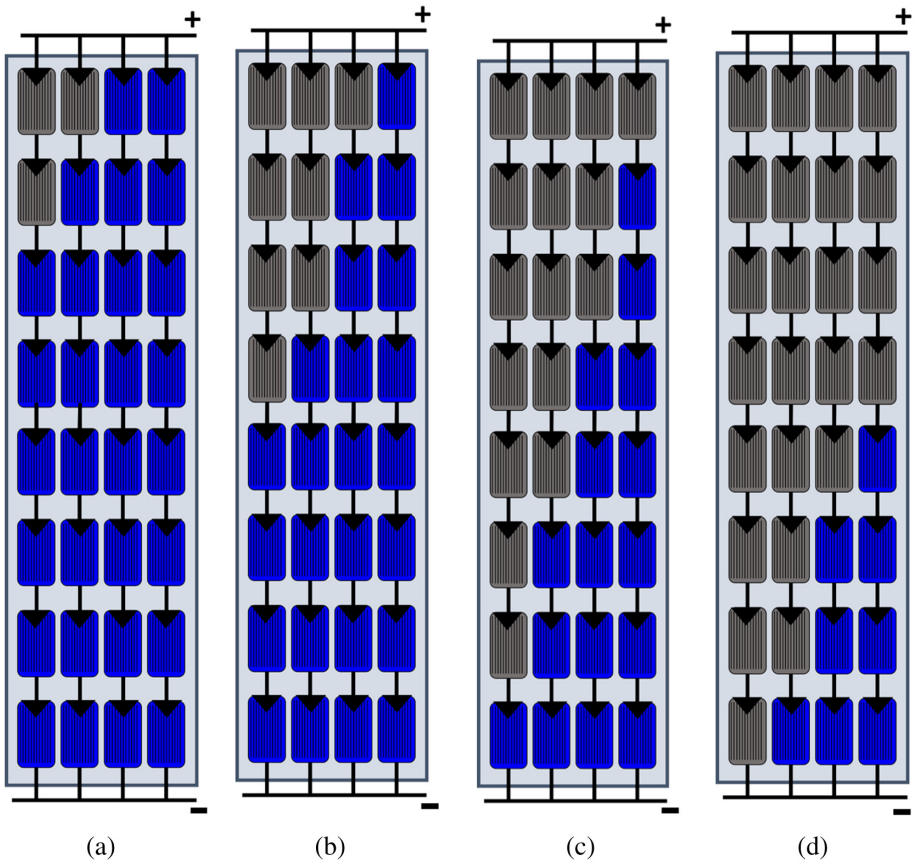

Fig. 6 Shading pattern used for the experiment: (a) 10% of shaded PV cells, (b) 25% of shaded PV cells, (c) 50% of shaded PV cells, and (d) 75% of shaded PV cells.

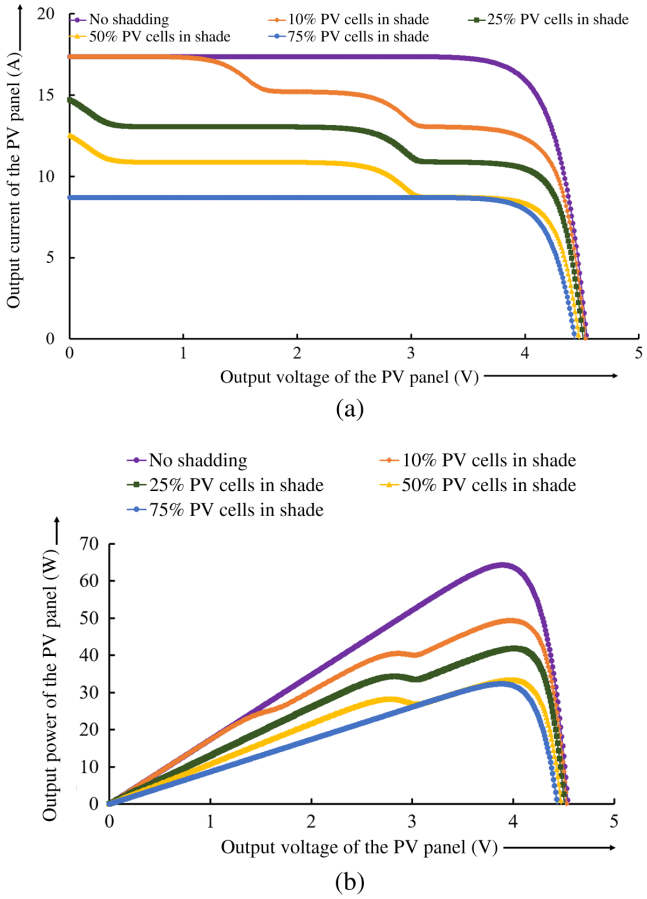

Fig. 7 (a) *I–V* characteristics of SP PV panel with 32 PV cells; (b) *P–V* characteristics of SP PV panel with 32 PV cells. The total number of PV cells in series is equal to 8, whereas the total number of PV cells connected in parallel is equal to 4.

The open-circuit output voltage of the PV panel, with 32 PV cells connected in 8×4, is equal to 4.54 V. The short circuit current for the same configuration is equal to 17.4 A.

4 Results

Since the total power generated by the PV panel is essential in determining the power efficiency, we evaluated the *P–V* characteristics for different topologies under 10%, 25%, 50%, and 75% partial shading conditions. The CMOS-embedded reconfigurable PV module can change its configuration by altering the number of PV cells in series and parallel. Therefore, unlike fixed topologies, SP, TCT, BL, and HC, their performance is tested for the entire possible configuration that gives out maximum power efficiency. The *P–V* characteristics of each case are shown in Fig. 8. As shown in Figs. 8(a)–8(c) for 10%, 25%, and 50% shading conditions, the TCT topology generates maximum power. However, for a 75% shading condition, maximum power is obtained with BL topology, as presented in Fig. 8(d).

It is clear from *P–V* characteristics shown in Fig. 8 that, among all the topologies, CMOS-embedded PV panel demonstrated a better capability of dealing with shading conditions. This is evident from the peaks of the curves in all the configurations we tested and shown in Fig. 8. It is apparent from Fig. 8 that CMOS-embedded PV panels generated maximum power when in 2×16 configuration. The maximum possible power generated by all the topologies for different partial shading pattern is shown in Fig. 9. It is evident from all four partial shading conditions that the most efficient way of dealing with partial shading is by reducing the total number of PV cells connected in series, since the current driving capacity of a series connected PV cells is

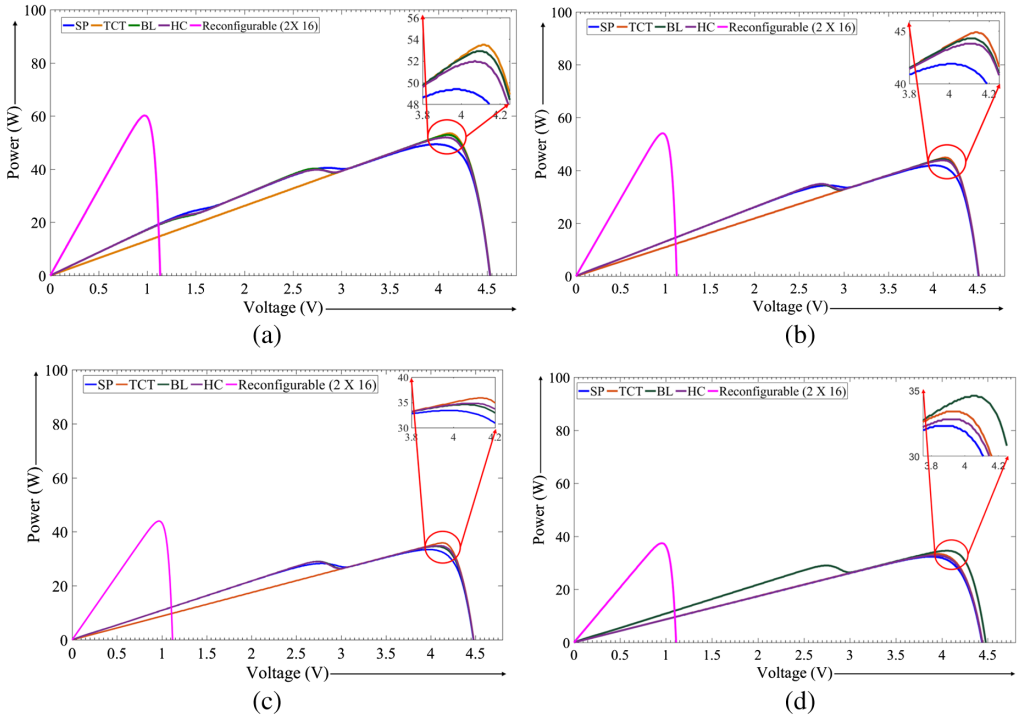

Fig. 8 The *P–V* characteristics of 32 PV cells-based PV panel for different shading patterns. (a) 10% of shaded PV cells, (b) 25% shaded PV cells, (c) 50 % of shaded PV cells, and (d) 75% of shaded PV cells.

determined by the least efficient PV cell in the row. The CMOS-embedded PV panels can smartly reconfigure the PV panel in real-time and reduce the impact of power loss due to shaded PV cells in series with unshaded PV cells.

Based on the results presented in Figs. 8 and 9, it can be concluded that a CMOS-embedded PV panel can deal with partial shading conditions by reducing the total number of PV cells connected in series. Therefore, every time a partial shading condition is detected, a reconfigurable PV panel will change to a configuration with a minimum number of PV cells in series. However, this reduction of PV cells connected in series can diminish the effectiveness of the reconfigurable PV array when the partial shading condition is changing in quick succession.

To address this concern, we measured the maximum power generated under 10%, 25%, 50%, and 75% for all topologies. Later, P_{max} is computed using Eq. (4) and is compared with the power generated by CMOS-embedded PV panel for various configurations under different partial shading conditions.

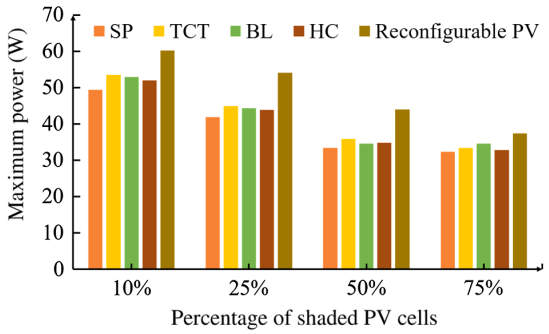

Fig. 9 Maximum power generated under various partial shading conditions was simulated using SPICE simulation. The reconfigurable PV panel is in 2 × 16 configurations, where 2 is the number of PV cells in series and 16 is the total of PV cells in parallel.

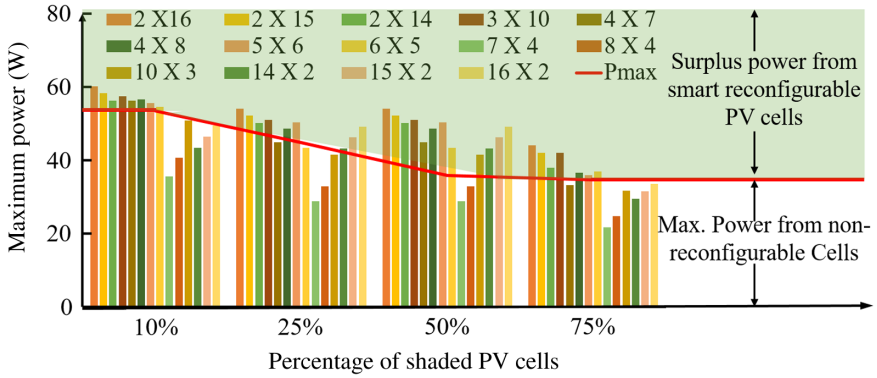

Fig. 10 Maximum power generated under various configuration (number of PV cells in series *X* number of PV cells in parallel) for different shading patterns by CMOS-embedded reconfigurable PV panel. P_{max} is the maximum power generated in fixed topology.

$$P_{max} = \max\left(P_{SP}, P_{TCT}, P_{BL}, P_{HC}\right). \tag{4}$$

In Fig. 10, P_{max} is the maximum power generated among fixed topologies for four different shading conditions. It is clear from Fig. 10 that a reconfigurable PV panel gives out many local maxima points that are better than other fixed (SP, TCT, BL, and HC) topologies. Hence, a reconfigurable PV panel is not required to reduce the total of PV cells connected in series to the minimum for outperforming the fixed topology PV panel under partial shading condition. From Fig. 10, for all four cases, the reconfigurable PV module generated maximum power when it is in 2×16 configuration. The schematic arrangement of reconfigurable PV module in 2×16 for all four shading conditions is shown in Fig. 11.

Thus far, for all the cases, we assumed the MOSFET transistors to be resistorless. However, that is not the case. These MOSFET transistors offer some resistance, which is called ON-resistance. Mostly, the ON-resistance can be reduced by increasing the aspect ratio (width per

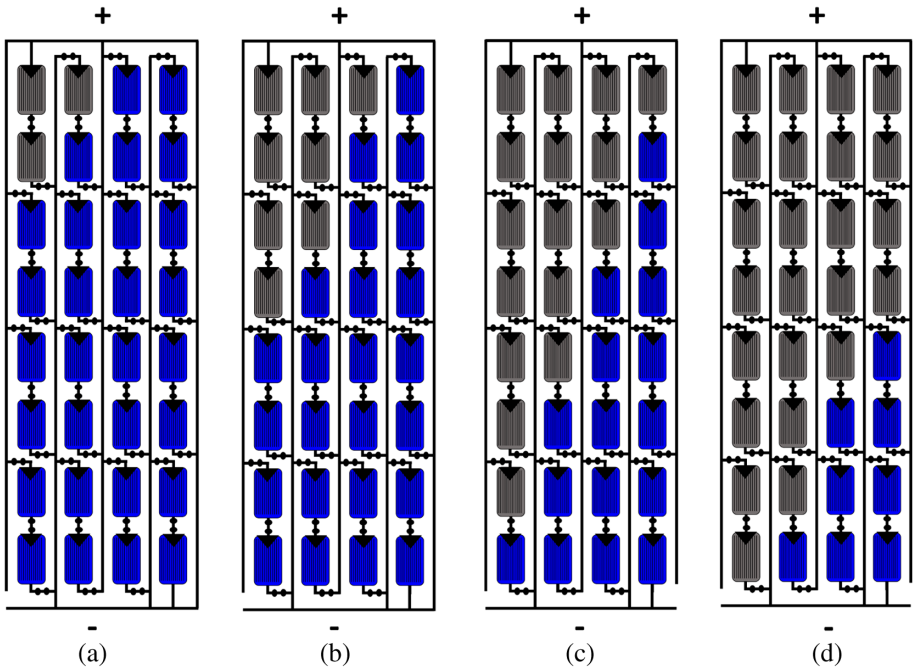

Fig. 11 The PV module embedded with CMOS-based APS switches is programmed to be in 2×16 configurations when (a) 10% of PV cells are shaded, (b) 25% of PV cells are shaded, (c) 50% of PV cells are shaded, and (d) 75% of PV cells are shaded.

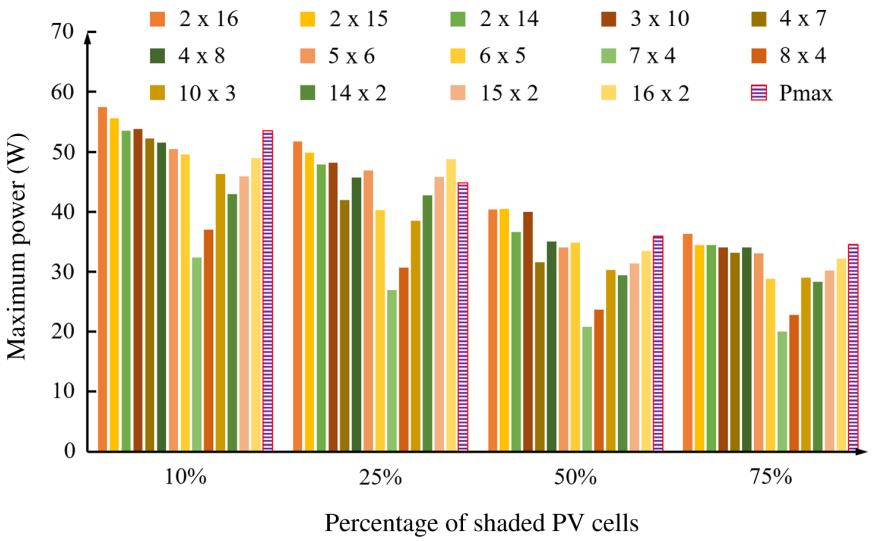

Fig. 12 Maximum power generated by reconfigurable PV module under various configurations for different shading conditions. The ON resistance of each MOSFET switches is equal to 11 mΩ.

length) of each MOSFET transistor. Still, the contact resistance of two-terminals of the MOSFET transistor plays an essential role in determining its ON-resistance. Therefore, a realistic comparison between the reconfigurable PV module with other fixed topologies is shown in Fig. 12. The ON-resistance of each MOSFET switch is equal to 11 mΩ.

In Fig. 12, it is seen that for all the four shading conditions, the reconfigurable PV module performance is still better than that of the fixed topology. However, compared to Fig. 10, the performance of the PV module in Fig. 12 is reduced due to the ON-resistance of the MOSFET transistor. Hence, for the reconfigurable module to be effective during partial shading conditions, the ON-resistance of the MOSFET transistors has to be minimal. The minimization of ON-resistance in a reconfigurable PV module can be achieved by creating monolithic CMOS-on-PV, as presented in Ref. 36. Besides offering lower resistance, a monolithic CMOS-on-PV module offers many advantages that are discussed in Refs. 36 and 39.

5 Discussion and Future Works

The traditional power grid is moving toward a smart grid, where there will be two-way communication between the customers and utility companies. This is envisioned to be achieved through IoT and 5G technology.[43] A smart grid will integrate renewable energy with the conventional power grid. Since the CMOS-embedded PV panels are integrable with IoT and 5G technologies, these have the qualities to eventually become part of smart grid systems. Also, when such a reconfigurable PV panel is deployed citywide and statewide, the combined power improvement by this smart panel will be quite significant. These reconfigurable PV panels can be ideal for the location where the area of installation is limited. Since this CMOS-embedded PV panel using the spatial and temporal tuning in the configuration can dynamically improve the overall power efficiency under changing irradiation conditions. Moreover, due to its ability to change the configuration according to the change in the solar irradiation. Hence, they are ideal to be deployed in places that are near to the northern hemisphere. Also, the increase in power production through CMOS-embedded PV systems will eventually reduce carbon emission and other related issues. As a result, this research is a good fit with the National Climate Assessment (NCA) report recommendations calling for researching adaptation and mitigation strategies to counter climate change.[44]

One of the critical components of the CMOS-embedded PV module is the algorithm.[32,33,37–39] The algorithm first detects the presence of partial shading conditions and then, based on the presence of shaded PV cells, determines the configuration that minimizes the effects of partial shading conditions.

For making the reconfigurable PV panel much smarter, the algorithm used by them should be sensitive enough to detect the presence of shaded PV cells in the panel. Also, the algorithm should have finality in determining the total presence of unshaded PV cells. Moreover, the algorithms should be fast enough to correctly determine the optimal configuration that can minimize the inefficiency created while changing from one configuration to the other. Therefore, the role of the algorithm is critical for the overall performance of CMOS-based smart PV systems; else the improvement in performance due to the reconfigurability will not be realized. Hence, more research work in improving the algorithm of the reconfigurable PV will make it even more revolutionary in powering technologies of the future.

6 Conclusion

In this paper, the effectiveness of fixed topology and reconfigurable PV panel under partial shading condition is compared. For a fixed topology, an SP with bypass diode, TCT, BL, and HC are used. For reconfigurable topology, a CMOS-embedded PV panel is used. The performance of each topology is analyzed and compared using SPICE modeling for four different partial shading conditions. Based on the *P–V* characteristics of each topology, the CMOS-embedded PV panels outperform other fixed topology-based PV panels. Reconfigurable PV panels provide a smart solution that can dynamically adjust to different configurations to outperform other fixed topologies in partial shading conditions.

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