Journal of Photonics for Energy

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REVIEW

Brief review of cadmium telluride-based photovoltaic technologies

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Abstract. Cadmium telluride (CdTe) is the most commercially successful thin-film photovoltaic technology. Development of CdTe as a solar cell material dates back to the early 1980s when ~10% efficient devices were demonstrated. Implementation of better quality glass, more transparent conductive oxides, introduction of a high-resistivity transparent film under the CdS junction-partner, higher deposition temperatures, and improved Cl-treatment, doping, and contacting approaches yielded >16% efficient cells in the early 2000s. Around the same time period, use of a photoresist plug monolithic integration process facilitated the demonstration of the first 11% efficient module. The most dramatic advancements in CdTe device efficiencies were made during the 2013 to 2014 time frame when small-area cell conversion efficiency was raised to 20% range and a champion module efficiency of 17% was reported. CdTe technology is attractive in terms of its limited life-cycle greenhouse gas and heavy metal emissions, small carbon footprint, and short energy payback times. Limited Te availability is a challenge for the growth of this technology unless Te utilization rates are greatly enhanced along with device efficiencies. [DOI: 10.1117/1.JPE.4.040996]

Keywords: photovoltaics; thin-film solar cell; cadmium telluride solar cell; cadmium telluride module integration; photoresist plug monolithic integration process.

Paper 14018MV received Mar. 27, 2014; revised manuscript received May 14, 2014; accepted for publication May 16, 2014; published online Jun. 27, 2014.

1 Introduction

For decades, the case for thin-film photovoltaics (PV) has been its low-cost potential. It was argued that inexpensive, large-area deposition methods could be developed to yield high-efficiency devices, and monolithic integration methods would lower the cost of module fabrication. Having achieved many of these targets, cadmium telluride (CdTe) is today the most commercially successful thin-film PV technology with a market share of ~5 to 6%. CdTe, with its near-ideal bandgap of ~1.5 eV and high optical absorption coefficients, was recognized to be a promising thin-film solar cell material back in 1950s.[1] But, it took researchers nearly three decades of R&D work to translate this potential into the first encouraging results when ~10% efficient devices were reported during the 1980–1985 period by groups using a variety of film growth techniques, such as screen printing,[2] close-space sublimation (CSS),[3] and electrodeposition (ED).[4] Then, yet another three decades of R&D effort was needed for the CdTe cell efficiency to reach the present 20.4% level[5] and for the CdTe module to become a strong competitor in the global PV market.

CdTe solar cells can be fabricated in superstrate or substrate configurations. As shown in Fig. 1(a), devices with the superstrate configuration are processed by forming a transparent-conductive-oxide (TCO)/junction-partner/CdTe/back-contact stack on a transparent sheet, i.e., superstrate, through which light enters the device. In the substrate configuration of Fig. 1(b), the deposition sequence is reversed and the stack is formed on a substrate, which does not have to be transparent. The highest-efficiency devices and commercialized modules have typically been fabricated using the superstrate configuration.

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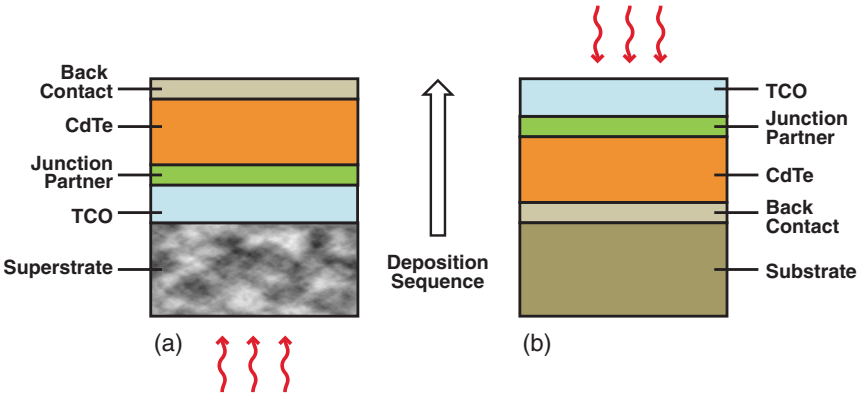

Fig. 1 CdTe solar cell configurations: (a) superstrate and (b) substrate.

Much of the early work on CdTe cells concentrated on film deposition techniques with the hope of finding one that can form the highest-quality absorber and junction. However, it became clear by mid-1980s that as-deposited CdTe films, irrespective of their deposition methods, did not produce efficient devices. Fabrication of efficient cells required certain postdeposition process steps that had to be applied to the already deposited CdS/CdTe film stacks.[6] These steps included annealing the stack at high temperature (>350°C) in presence of Cl, treating the CdTe film to render its exposed surface Te-rich, and introducing a dopant, such as Cu and Hg, at the Te-rich surface before or during back-contact formation. During the 1990s, optimization of the Cl-treatment/contacting/doping processes yielded an impressive 15.8% cell.[7] In the 2000–2002 period, there were two important developments. First, the champion cell efficiency was improved to 16.7%[8] as a result of higher temperature absorber film growth, a highly transparent cadmium stannate (CTO) layer as TCO, and successful implementation of zinc stannate (ZTO) as a high-resistivity transparent (HRT) layer[9] at the TCO/CdS interface. Second, a module manufacturing process based on the ED CdTe technology[10] was demonstrated by BP Solar, yielding a nearly 11% large-area module.[11] During the decade following these developments, the effects of the postdeposition processes on device performance were better understood and the vapor transport deposition (VTD) technique,[12] which can form layers on fast-moving substrates, was further optimized by First Solar, eventually becoming the most commercially successful approach. A detailed discussion of the early CdTe technology development can be found in Ref. 13. Fundamental materials properties, device physics, and modeling aspects are presented in detail in Ref. 14. In this paper, we will summarize some recent results that contributed to a better understanding of the cell fabrication processes. We will also review some of the topics that are important for CdTe PV, such as module integration, Te availability, and life cycle profile.

2 Processing of Cells with Superstrate Configuration

Typical process steps for fabricating a CdTe thin-film cell with superstrate configuration include deposition of a TCO layer, formation of a CdS/CdTe stack over the TCO layer, Cl-treatment, cleaning of the CdTe film surface, doping, and formation of a back-contact. As a polycrystalline device, performance of a CdTe cell is dominated by surfaces, such as grain boundaries and film interfaces, that get affected by every one of the above listed process steps to various degrees, depending on the as-deposited properties of the layers within the cell stack.

2.1 *Superstrates*

Low-cost soda-lime glass was employed as the superstrate in some of the early 10% efficient cells. However, the strain point of this glass is only ~515°C and its optical transmission is <80% for wavelengths <450 and >700 nm,[15] an issue that can be mitigated by reducing the iron content to or <200 ppm. In fabricating the champion cells, R&D groups often employ more expensive but highly transparent glasses with high strain point. For example, the 16.7% cell employed

a thin borosilicate glass and a process temperature that reached 660°C.[16] Therefore, there is continued effort on the part of suppliers to engineer a high-temperature, high-transparency glass, which is also stronger so that superstrates much thinner than the standard 3.2 mm can be used in module fabrication.[17] Such superstrates, once available at low cost, are expected to yield higher efficiency, lighter-weight commercial CdTe modules. The above-mentioned 16.7% cell also employed a single-layer antireflective (AR) coating on the glass surface.[16] A recent study demonstrated that a multilayer AR coating can reduce the weighted average reflection of the glass surface from ~4 to ~1% within the absorption band of CdTe.[18] Use of AR coatings in commercial modules requires development of cost-effective and environmentally durable films. Information such as the nature of the glass and the AR coating (if any) has not been disclosed for the recently reported champion devices (see Secs. 2.5 and 4.1). However, it would be reasonable to assume that they employed the best quality glass available and possibly an optimized AR coating.

Another topic that attracted recent attention is luminescent down-shifting,[19–21] which uses a luminescent down-shifting (LDS) material layer on the cell surface to shift the wavelength of high-energy ($\lambda < 500$ nm) photons to values around ~600 nm. This approach was shown to increase the current density in cells with relatively poor blue response; however, long-term stability and cost aspects of LDS materials are uncertain. Also, the efficiency improvement provided by this approach would diminish as the blue response of the cells is improved through advances made in optical transmission and/or current collection from the glass/TCO/junction-partner stack.

Although glass is the most economical and proven superstrate material, a thin (~7.5 μm) transparent polyimide foil was also used to demonstrate a flexible CdTe cell. All the layers in this polyimide/ZnO/CdS/CdTe/back-contact device were processed at temperatures <450°C and an efficiency of 12.7% (with AR coating) was reported.[22]

2.2 *TCO/Junction-Partner Stack*

All high-efficiency CdTe cells utilize a thin HRT film between the TCO and CdS layers. Although a wide range of material options and thicknesses have been used to reach cell efficiencies in the 10 to 15% range, a down-selection of the cell stack and the processing options has emerged, which produces efficiencies >15%. For high efficiency, the junction is typically formed at temperatures near 600°C, limited by the strain point of the glass and the impurity diffusion from the glass into the CdTe absorber. There is typically a diffusion barrier layer (a thin SiO_2 film) at the glass/TCO interface to control such diffusion. The window stack utilizes several index-matched layers to (1) reduce reflection, (2) maximize transmittance, (3) control lateral conductivity for current collection, (4) passivate CdTe and form a low-recombination junction, and (5) serve as a CdTe nucleation surface with high in-plane density, low voiding, and low extended defect CdTe growth. For this, fluorine-doped tin oxide and CTO, both of which are stable at temperatures up to ~620°C, have been employed as TCO layers. Typical TCO films are 0.25 to 0.7 microns thick and exhibit sheet resistance in the 5 to 15 ohm/sq range, with CTO films exhibiting cross-grain mobilities of >60 $cm^2/V\text{-}s$ and a carrier density of $\sim 10^{19}/cm^3$. An HRT film is deposited on the TCO as a buffer layer to reduce leakage current and improve CdS film quality. Undoped tin oxide and ZTO (or Zn-doped tin oxide) have been successfully used as HRT layers at thicknesses in the 30-nm range. Since CdS typically does not contribute photocurrent to the cell, its 2.4-eV bandgap causes parasitic absorption at wavelengths <500 nm, and for this reason, its thickness needs to be reduced as much as possible. CdS can be deposited by numerous methods, including VTD, CSS, sputtering, and chemical bath deposition. Incorporating oxygen into the CdS film[16] during growth improves CdS film durability[23] to high CdTe deposition temperature by reducing vapor pressure and diffusivity, allowing ultrathin CdS films to be employed, with final thickness being <30 nm.

2.3 *Cl-Treatment*

As-deposited CdTe films contain extended and point defects and are of poor electronic quality. For example, VTD CdTe films formed at 580 to 600°C at a rate of 10 μm/min exhibit grains

with 1:1 aspect ratio, and weak p-type conduction with low mobility and low carrier concentration of $<10^{14}/cm^3$. Time-resolved photoluminescence (TRPL) analysis of such films at the CdS interface showed a minority carrier effective lifetime of <1 ns.[24] In another study on CSS grown CdTe layers, a high grain boundary recombination velocity of $\sim 10^4$ cm/s was recently estimated from the cathodoluminescence data.[25]

Following the CdTe deposition step, the entire film stack is subjected to a thermal treatment at a temperature around 400°C in the presence of $CdCl_2$ and oxygen. This treatment drastically reduces CdTe extended defect density, increases p-type conductivity (acceptor density reaching $10^{14}/cm^3$ level), and passivates the grain surfaces, increasing the effective minority carrier lifetimes to >3 ns. It should be noted that a TRPL second decay constant (which is related to lifetime)[26] of 10 to 15 ns was recently reported for the 18 to 19% efficient devices.[27] High temperature deposition, Cl-treatment, and grain boundary diffusion promote interdiffusion at the CdS/CdTe interface and convert this interface into a $CdS_{1-y}Te_y/CdTe_{1-x}S_x$ junction, where the values of x and y depend on the temperature reached and are typically $x \sim 0.05$ and $y \sim 0.03$. Alloying reduces the lattice mismatch at the junction from ~11 to ~9% and decreases the energy gap slightly on each side of the junction due to the optical bowing parameter induced by nonideal mixing.[13]

2.4 *Doping and Contacting*

Cl-treatment leaves a mixture of native oxides (CdO, $CdTeO_3$, $CdTe_2O_5$) and Cd- and Te- oxychlorides on the CdTe surface. After removing these residues, a Cu source layer is typically deposited on the clean surface and the dopant is driven into the CdTe layer through moderate annealing. Copper source layers include Cu-doped graphite paste and low-resistivity compounds, such as Cu_2Te and Cu-doped ZnTe, that form low-resistance primary contacts with contact potential barriers <0.3 eV. Amount of Cu introduced is critical and has an optimum value based on the device structure[28] and the nature of the CdTe layer. After the doping step, high-efficiency devices are reported[27] to have an ionized acceptor density in the range of 0.5 to $1 \times 10^{15}/cm^3$. A large volume of literature exists on the role of Cu in CdTe solar cells, including its interaction with defects, its distribution in the cell structure, and its influence on minority carrier lifetime and cell stability. The reader is referred to Refs. 29 and 30 for a recent discussion of some of these topics. After the doping step, a robust secondary contact is deposited over the primary contact layer to facilitate lateral current collection. The secondary contact may be a single metal film, such as Au, Ni, or Mo, in the laboratory devices; however, for longer-lifetime contacts, a diffusion buffer layer may first be deposited. Nitrides of refractory metals, such as MoN and TiN, act as good barriers. Once the barrier is deposited, lower-cost metals, such as Al, can be used for lateral conduction. MoO_x has recently been investigated as a high work function buffer layer in CdTe cell contacts.[31]

2.5 *Recent Superstrate Cell Results*

Recent progress in CdTe cell efficiency has been rapid.[27] In 2011, First Solar announced a 17.3% efficient cell. Then, in 2012, GE Global Research Center (GE) revealed a verified 18.3% efficient device, which was followed by an 18.7% cell by First Solar. In early 2013, GE announced a 19.6% device. In mid-2013, First Solar acquired the GE technology and, in 2014, announced a new champion cell with 20.4% efficiency.[5] Current–voltage characteristics of the 18.7% device and the quantum efficiency (QE) data for the 17.3, 18.3, and 18.7% devices can be found in Ref. 27 [also see Fig. 2(a) below]. Parameters of the 19.6% device[32] were $V_{oc} = 857.3$ mV, $J_{sc} = 28.59$ mA/cm^2, FF = 0.80. Unfortunately, there are no details about these highly efficient devices. However, improvements in efficiency seem to be marked by gains in J_{sc}, most probably by modification of the glass type/thickness, an optimized AR coating as well as modifications to the window layer stack to achieve more optical throughput. It should be noted that the J_{sc} value of the 16.7% device from National Renewable Energy Laboratory (NREL) was 26.1 mA/cm^2, whereas this value is improved to 28.59 mA/cm^2 for the recent 19.6% efficient cell. The voltage improvement was only ~12 mV.

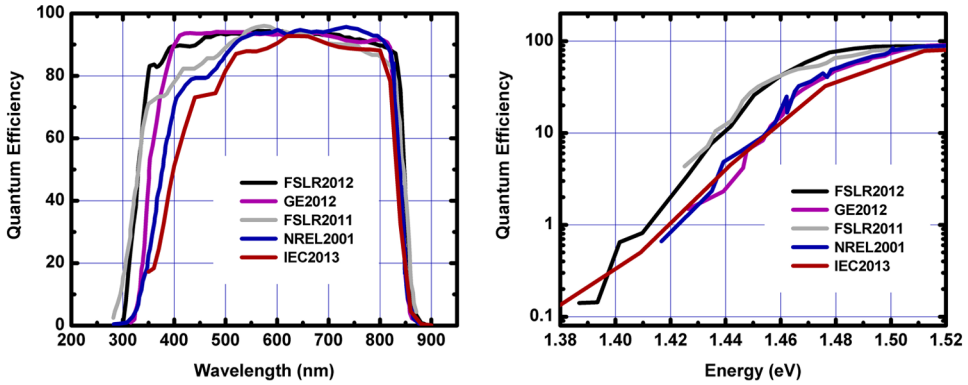

Fig. 2 (a) Quantum efficiency (QE) versus wavelength comparison of five different cells. (b) $\log_{10}$ QE versus energy data for the cells of (a).

The QE of Institute of Energy Conversion (IEC) 2013 (16%), NREL 2001 (16.7%), First Solar 2011 (17.3%), and GE 2012 (18.3%) devices are compared in Fig. 2(a), where the QE is plotted over the entire range of wavelengths, and in Fig. 2(b), where $\log_{10}$QE versus energy relationship near the absorber band gap is shown. The IEC cell employed a Corning engineered low-sodium glass, a ZTO/CTO stack, and a 60-nm-thick CdS layer. The impressive J_{sc} improvement in the GE device is due to the refinement of the window stack, increasing the UV and blue response, resulting in a square QE from the glass cutoff to the CdTe band gap. It is clear that the higher current densities of the other cells in Fig. 2(a) are also due to more transparent window, First Solar cells reaching deeper into the UV region. At 1.5-eV cutoff, the maximum AM1.5 photocurrent for CdTe is ~30.5 mA/cm^2. To get closer to the practical current density goal of 30 mA/cm^2, one can use even thinner and more transparent glass superstrate and/or narrow the CdTe band gap so that the long wavelength response extends ~15 nm more, potentially adding another 1 mA/cm^2 to the current. One way of reducing the bandgap of CdTe is to alloy it with CdS and/or CdSe. Although both of these materials have higher bandgap values than CdTe, the $CdTe_{1-x}S_x$ and $CdTe_{1-x}Se_x$ alloys display bandgap values smaller than CdTe for x values $\ll 0.1$. For the case of S, an x value of ~0.03 would be adequate for 15-nm extension of the QE. For the case of CdSe, an x value of ~0.05 would be adequate. It should be noted that $CdTe_{1-x}Se_x$ crystals have enhanced charge transport properties compared to CdTe crystals,[33] and the lattice constant of CdSe (6.05 Å) is between CdS (5.83 Å) and CdTe (6.48 Å). Use of a Cd-Se-S or CdSe/CdS junction-partner would allow alloying of the CdTe absorber with both S and Se during the $CdCl_2$ treatment step and reduce the lattice mismatch further.

3 Processing of Cells with Substrate Configuration

Attaining high efficiency for CdTe cells in the substrate configuration is challenging. This device design requires formation and retention of a low-resistance back-contact while obtaining a high-quality CdTe film and junction. The problem for CdTe is the fairly high hole affinity of ~5.8 eV, which requires a very high work function contact material. In the superstrate cell structure, the junction is formed at high temperature and is passivated by alloying between the CdS and CdTe as described in Sec. 2.3 above, and the back surface is available for chemical manipulation to tailor the contact properties. In the devices with the substrate configuration, although the collecting junction surface is available for manipulation, the back-contact is sequestered and subject to degradation during the following high temperature steps. Recently, a cell with 11.3% efficiency was demonstrated[34] with the configuration of substrate/contact/buffer layer/CdTe/CdS/TCO. This device employed a borosilicate glass substrate, an Mo contact, and a $Cu/Te/MoO_3$ buffer layer stack, and the process temperatures were kept <400°C. Devices made on metallic foil substrates have so far yielded <10% efficiency.

4 Modules

4.1 *Recent Module Results*

After the demonstration of the first 11% CdTe module in 2000,[11] the biggest jump in efficiency came in early 2012 when First Solar reported a 14.4% efficient device. In early 2013, the efficiency was improved to 16.1%, and a 17% (17.5% aperture area) module was announced[35] in March 2014. QE data of the 16.1% module[32] show appreciable current loss in the UV-blue region of the spectra compared to the high-efficiency cells reported around the same time. Clearly, the stack used in the module was different from the one in the cells. No data are yet available about the 17% module to see where the improvement came from. The details of the champion module process flow are important to be able to assess how the large gap between the champion cell efficiencies (~20%) and the efficiencies of the commercial modules (13 to 14%) can be reduced without increasing cost of manufacturing appreciably.

4.2 *Monolithic Integration*

There are two monolithic integration methods that have been employed in CdTe module fabrication. In the first approach[36] shown in Fig. 3, the process flow includes deposition of a TCO layer, formation of the P1 scribe lines, deposition of the CdS/CdTe stack, formation of the P2 scribe lines, deposition of a back-contact, and formation of the P3 scribe lines.

Diode pumped solid-state lasers with nanosecond pulses are commonly used for the scribing steps,[37] and the laser beam preferably enters from the glass side. For ~50-μm-wide scribes and 50 μm distance between them, the total width of the dead zone in Fig. 3 can be in the order of 250 to 350 μm, taking into account the heat-affected areas and the inaccuracies in positioning and parallelism. For a 10-mm-wide cell, this corresponds to a current loss of ~3%. Obviously, there have been ongoing efforts to reduce the scribe widths to <25 μm and to decrease the size of the dead zone.[38] The possibility of shunting through the CdTe bridge is a shortcoming of this method. Shunting may result from defects in the bridge area due to poor nucleation and growth of the CdS and/or the CdTe layer(s) onto the exposed glass surface and due to impurity diffusion from glass and impurity accumulation during the processes described in Secs. 2.3 and 2.4. For a technology like ED, it is not even possible to grow a uniform CdTe layer at or around the P1 scribe lines because of lack of a highly conductive surface underneath.

In an alternative integration approach[39] that was employed in early modules,[40] a TCO/CdS/CdTe stack is first deposited and then the P1 scribe lines are formed through the whole stack. Then a resist is dispensed into the P1 lines. The process continues with the formation of the P2 scribe lines, contact deposition, and the formation of the P3 scribe lines. The challenge with this integration technique is dispensing a resist into a large number of P1 scribe lines in a fast, repeatable, and economical manner without leaving any uncovered area that would later cause a shunt, while trying to minimize the area of the dead zone. This important problem was overcome by the development of a photoresist plug integration process, which has been very successful.

The photoresist plug integration process was developed by Basol[41] and applied to cells and small submodule circuits fabricated by the ED technique[10] at Monosolar. The idea was to indiscriminately fill any opening in the electroplated CdS/CdTe stack with an insulating resist rapidly and with ~100% yield. The process was later transferred to BP Solar and used for the fabrication of the 11% module,[11] although the details of this process was not published. As shown in Fig. 4(a), the first step in the photoresist plug technique is deposition of a TCO/CdS/CdTe

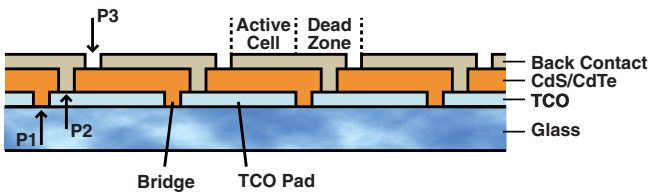

Fig. 3 Module structure with a CdTe bridge between transparent-conductive-oxide (TCO) pads.

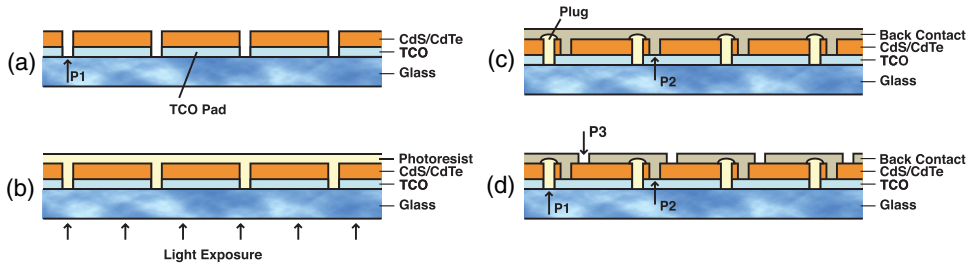

Fig. 4 Photoresist plug integration process flow for monolithic integration: (a) deposit TCO/CdS/CdTe stack and form P1 scribe lines, (b) cover the surface with photoresist and expose through the glass superstrate, (c) develop and rinse forming the photoresist plugs, form P2 scribe lines, deposit back contact, (d) form P3 scribe lines.

stack followed by the formation of the P1 scribe lines. Then a negative photoresist material is coated over the surface, filling the P1 scribe lines as shown in Fig. 4(b). The next step is light exposure through the glass, which results in the exposure and cross-linking of the resist within the P1 scribe lines. The CdTe film, acting as an opaque mask, protects the resist layer at the top surface from getting exposed. Treating the structure by a resist developer removes the unexposed resist from the CdTe surface and leaves the hardened photoresist plugs in the P1 scribe lines only. The process may then proceed through the formation of the P2 scribe lines and the deposition of the back-contact [Fig. 4(c)]. Final device structure is obtained after the formation of the P3 scribe lines [Fig. 4(d)]. The monolithically integrated module structure of Fig. 4(d) has many advantages and, to the best of the authors' knowledge, is the approach that has been widely adapted, with vendors offering in-line systems to carry out the photoresist deposition (by spraying or rolling), exposure, development, and rinse steps. The resist plugs in Fig. 4(d) do not allow any shunts between the TCO pads irrespective of the CdTe resistivity or the scribe line width. Furthermore, the height and shape of the plugs can be manipulated by adjusting the viscosity/thickness of the photoresist and the exposure time/intensity. For example, mushroom-shaped plugs, which can insulate the damaged region around the P1 scribe lines, can be formed by using thicker resist layers and longer exposure times. Through such optimization, the photoresist plug integration process minimizes the dead zone while providing good electrical isolation. It also passivates any pinholes that may be present within the cells.

4.3 *Field Performance of Modules*

CdTe is a relatively new PV product. Although indoor and outdoor stability tests of early modules and small systems have been carried out for many years,[42,43] deployment of commercial modules in relatively large fields has only about a 10-year history. While efforts are underway to increase the CdTe performance as measured under standard test conditions, it is also essential to model the behavior of these devices under real deployment conditions in various geographical locations. A recent indoor study of the effect of temperature on power output of modules showed a temperature coefficient of −0.21%/°C for CdTe compared to −0.45%/°C for Si.[44] Another report on modules deployed outside in Spain showed an average temperature coefficient of −0.35%/°C, which varied widely between summer and winter months[45] due to the effect of solar spectrum variation on the energy yield of CdTe.[46] In another outdoor study,[47] the annual average daily yield of CdTe modules (~5.4 Wh/Wp) was found to be somewhat higher than poly-Si modules (~5.3 Wh/Wp) and the daily efficiency decreases were smaller for CdTe (~5.4%) compared to poly-Si (7.6%) since modules operated mostly under high irradiation conditions. Janke and Strasser,[48] however, could not confirm higher yields for CdTe modules in their measurements. Comparison of the DC performance loss rates for 12 different grid connected systems operated in Cyprus showed that the average annual performance loss rate for the CdTe modules of vintage 2006 was ~2.3%.[49] It is clear that much more data is necessary to improve the models for predicting the energy yield of a CdTe system, especially since the technology itself has been continually changing and some of the results quoted above were obtained using old vintage modules. Other phenomena, such as transient effects in modules,[50,51] also need to be further studied.

5 Life Cycle Profile and Te Availability

Environmental impacts and perceived risks of manufacturing and deploying CdTe modules have been a subject of much interest because of the relative success of this technology in the market and the presence of Cd in the cell structure. An excellent review of topics such as the life-cycle greenhouse gas emissions, energy payback times, pollutant and heavy metal emissions, and life cycle risk analysis of CdTe systems and their comparison to other PV technologies can be found in Ref. 52. In this study and others,[53] CdTe technology was found to have the shortest energy payback time (~0.8 years) and lowest emissions of all PV technologies. Kim et al.[54] estimated the carbon footprint of a CdTe-based ground mounted system to be $14gCO_2/kWh$ compared to 20 and $26gCO_2/kWh$ for a-Si and copper indium gallium selenide (CIGS) based systems, respectively.

With the recent dramatic growth of the world PV market and the optimistic projections for future growth, the question is often asked if CdTe can adequately participate in this growth considering the fact that Te is a rare material. A recent study by Houari et al.[55] provided an extensive review of the past literature on this subject and, through a system dynamics model, examined the effect of Te availability on the growth of CdTe technology by 2050. Without taking into account possible effects of Te price on production, and assuming continuous improvements in Te recovery rate, module efficiency, CdTe layer thickness, and Te utilization rate, the model predicted that it is possible to have enough Te available for a manufacturing volume of ~150 GW/year in 2050. Woodhouse et al.[56] examined the sensitivity of the module manufacturing cost to a 10-fold increase in the price of Te. They found that it was essential to improve the Te utilization rate to be able to keep the CdTe film cost at a 0.15/W level. It was projected that the manufacturing cost of CdTe modules would be 0.59/W at a high Te price of 3500/kg, provided that 18% efficient modules can be fabricated using only 1-μm-thick absorber.

As can be seen from the discussion above, development of a thin and highly efficient device is very important for future growth of the CdTe technology. There are challenges in processing cells with the standard structure but with only ~20 to 30% of the standard absorber thickness. First of all, the reduced absorptivity of the thin layer results in current loss. Second, bringing the back-contact closer to the rectifying junction is expected to increase the recombination losses. On a practical note, thinner films are more prone to pinhole generation, especially if they are grown at high temperatures, although this problem may be overcome by using the photoresist plug method of Sec. 4.2. Devices with absorber thicknesses in the range of 0.8 to 1.15 μm have recently been fabricated by evaporation,[57] low-temperature CSS,[58] and sputtering[59] techniques, yielding efficiencies of 9, 9.5, and 12.9%, respectively. An 11% efficient device with only 0.5-μm-thick CdTe absorber was also demonstrated.[59] A new CdTe cell design employing an electron backreflector was modeled to show its potential for >19% efficiency.[60] Although this is a very promising design theoretically, no successful experimental result has yet been published on such a device.

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