Experimental and simulation study of fill-factor enhancement using a virtual guard ring in n^+/p-well CMOS single-photon avalanche diodes

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Abstract. The use of a physical guard ring in CMOS single-photon avalanche diodes (SPADs) based on n^+/(deep)p-well and p^+/(deep)n-well structures is a common solution to control the electric field of the SPADs periphery and prevent the premature lateral breakdown. However, this leads to a decrease of the detection efficiency, i.e., the fill-factor, especially when the SPADs size is reduced. Our paper presents an experimental and simulation study on replacing the physical guard ring by a virtual guard ring to improve the fill-factor and the scalability of a n^+/p-well SPAD implemented in 0.35-μm pin-photodiode CMOS technology. Accordingly, the optimization of the virtual guard ring and its superiority at downscaling are discussed, and the SPAD scalability in size with respect to the fill-factor is quantified in this technology. [DOI: 10.1117/1.OE.60.6.067105]

Keywords: single-photon avalanche diode; virtual guard ring; scalability; fill-factor.

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1 Introduction

Detecting weak optical signals is critical to a variety of opto-electronic applications, including time-of-flight sensors, quantum cryptography, optical wireless communication, and optical tomography in medical diagnostics. This makes the single-photon avalanche diode (SPAD) an attractive candidate as it has a sensitivity level of detecting single photons.[1–4] The SPAD operation can be thought as a simple diode with a reverse bias above its breakdown voltage and therefore, an absorbed photon generates an electron–hole pair, which might gain enough energy to create a self-sustaining avalanche due to a strong electric field formed in a multiplication zone. The self-sustaining avalanche has to be stopped by reducing the voltage to below breakdown by a quenching circuit (active or passive) and then needs to be recovered (reset) for the next detection.

Si-CMOS SPADs based on n^+/(deep)p-well and p^+/(deep)n-well are commonly used structures with the capability to be integrated with circuitry.[5–8] In these structures, a physical guard ring was used to avoid a premature edge breakdown due to locally concentrated electric field at the edge of the junction. A variety of different physical guard rings, including diffusion guard ring,[9] trench isolation guard ring (STI),[10] and low-doped guard ring,[11,12] have been used to decrease the peripheral electric field at the edge of the junction. Nevertheless, the existence of the physical guard ring degrades the fill-factor defined as the ratio of the photo-sensitive area (active area) to the total device area. As it is shown here, this degradation is more significant when the SPAD is downsized and the dimensions of the guard ring are comparable to the dimensions of the photo-sensitive area.

To address this issue, a virtual guard ring has been employed in p^+/n-well SAPDs to achieve smaller structures.[13–16] In Refs. 13 and 16, the virtual guard ring is exploited between active area and STI to separate the edge of the STI from the avalanche region to reduce the dark count rate

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(DCR) induced by STI interface traps, which limits the fill-factor. However, in SPADs with a deep multiplication region, the combination of the virtual guard ring and STI is efficient in downsizing the SPAD as studied in Refs. 15, 17, and 18. Reference 19 presents different deep virtual guard ring structures to be used in SPADs with a deeper multiplication region in p^+/deep n-well CMOS SPADs. Here, we employ this concept in the n^+/p-well CMOS SPAD structure with separate thick absorption and multiplication zones, which is efficient for longer wavelengths for the first time. The effect of a virtual guard ring replacing a physical guard ring on the built-in electric field and the fill-factor of the SPAD is studied. Furthermore, we demonstrate that the lateral electric field at the edge of the active area decreases the effective active area due to the deviation of the carrier path from their pure vertical trajectory toward the boundary out of the multiplication region. To the best of our knowledge, the previous studies have not considered this effect; however, it is critical in scaling down our SPAD. Here, the Geiger mode simulation is performed to investigate the electric field behavior inside the structure and evaluate the effective active area. Furthermore, we measure experimentally the radial dependency of the photon detection probability (PDP) defined as the probability that an incident photon is detected to determine the active area (i.e., the fill-factor). In addition, the effect of the virtual guard ring on the parasitic noises, including the DCR and afterpulsing probability (APP), and the breakdown voltage (V_{br}) as the key performance factors of the SPAD are studied.

A good agreement between the simulation and the experimental results is achieved for large SPADs of both structures. Then, the structure of a smaller SPAD with a virtual guard ring within the same CMOS technology is designed based on simulations and is fabricated, accordingly.

The remainder of the paper is organized as follows. In Sec. 2, the structure of the SPAD with physical and virtual guard rings is described. Section 3 compares the simulation and experimental results for larger SPAD structures of both guard ring types. Section 4 studies the downscaling effect on the fill-factor for both SPAD structures and finally, the paper is concluded in Sec. 5.

2 Device Structure and Measurement Setup

2.1 *Device Structure*

Figure 1 shows the cross-sections and the top view of the circular SPAD structures fabricated in the 0.35-μm modular sensor technology platform (XO035) of X-FAB semiconductor foundries. Both SPADs include a shallow n^+ and p-well regions formed on a p-doped epitaxial layer (p-epi) with a doping concentration of $\sim 2 \times 10^{13}$ $1/\text{cm}^3$ and a thickness of ~ 12 μm. In both structures, the diameter of the n^+ and p-well are 90 and 80 μm, respectively.

When the SPAD is reversely biased above its breakdown voltage (operating in Geiger mode), a strong electric field is established at the n^+/p-well junction that serves as an avalanche

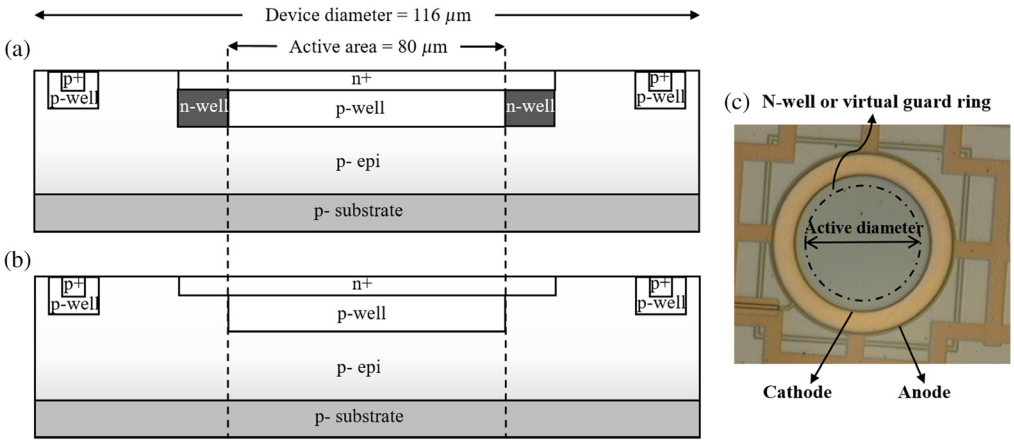

Fig. 1 Schematic cross-section (not to scale) of CMOS SPADs based on n^+/p-well structure with (a) the physical guard ring (SPAD1) and (b) the virtual guard ring (SPAD2). (c) Top view of these SPADs (there is no difference in the chip photos of both SPADs visible).

multiplication zone. At this voltage level, the depletion region extends down to the substrate, which means the whole epitaxial layer is depleted. Accordingly, the p-epi layer serves as a thick absorption zone, which makes the SPADs efficient to detect long wavelengths to be used in optical wireless communication systems and LIDAR/ToF sensor applications.

The only difference between these two SPAD structures is the form of the guard ring, which is necessary to avoid the curvature effect of the p–n junction and the formation of higher electric field at the edges resulting in a local edge breakdown. In SPAD1 [Fig. 1(a)], an n-well region (which is much lower doped than the n+ region) with a width of ~5 μm (here, after called physical guard ring) is present from the edge of the p-well to the edge of the n^+ region as it has been used in our previous SPADs.[3,20] In SPAD2 [Fig. 1(b)], the guard ring is made virtually as the diameter of p-well is less than that of the n^+ region so that the edge of n^+ region is surrounded by the low doped p-epi. Therefore, the electric field at the diode junction of n^+/p-well in the central region (including, the whole p-well) is higher than the peripheral electric field at the edges, and accordingly the central region reaches the breakdown voltage point earlier. As a result, the edge breakdown is avoided and the multiplication region is confined over the n^+/p-well junction. However, the use of these guard rings influences the built-in electric field and reduces the effective active area. A closer look into this effect using TCAD simulations and experimental measurements is presented in the following section.

2.2 *Measurement Setup*

The measurement setup is illustrated in Fig. 2. As laser source, a fiber coupled to a laser diode from Thorlabs is used (LPS-PM635-FC). We use two optical power meters in our setup. A fiber splitter is used to split up the light to feed it to the first optical power meter from Thorlabs for power monitoring (PM_{ref}) and to the fiber that feeds the light either to the device under test (DUT) or to the detector of a second power meter PM_{cal}. With attenuator Att2, the ratio between the optical power is set between the fiber that feeds the light to the DUT and the fiber that leads to the power monitoring. This ratio is set in the range of 10^5. For calibrating this ratio, the second power meter PM_{cal} is used that has a detector placed inside the dark box where the DUT is mounted. This high ratio guarantees that we get sufficient optical power at the power monitoring, when the photon rate at the DUT is set to 10×10^6 photons/s. Attenuator Att1 is used after calibrating the power ratio to reduce the photon rate at the SPAD. This light intensity is sufficiently low that any saturation and pile up effects are not observed. The setup is controlled by a PXI system. A digitizer (NI PXIe-5162) reads the output signals of the active quenching circuit (explained in detail in Ref. 20) and streams the data directly to an FPGA card (NI PXIe-7972R),

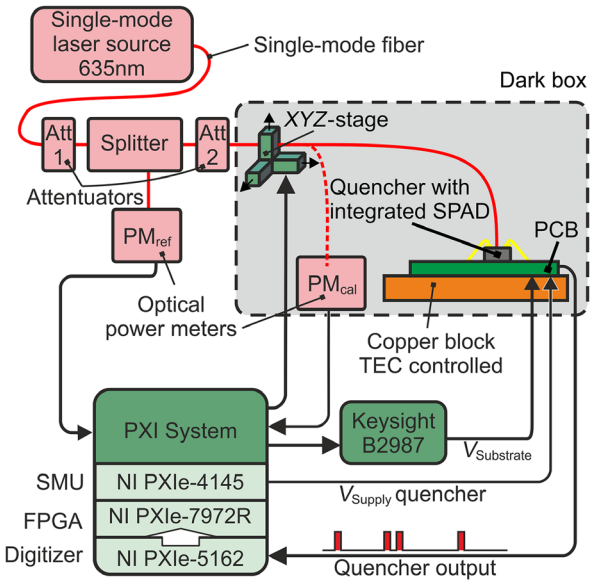

Fig. 2 Schematic of the measurement setup.

where the pulse statistics such as count rate and after pulsing probability are extracted. The active quenching circuit is supplied by an SMU card (NI PXIe-4145), and the substrate voltage is generated by a Keysight electrometer (B2987). The DUT's temperature is kept constant at 25°C by means of a thermo electric cooler. An XYZ-stage from Thorlabs built from three linear stages (KMTS50E/M) positions the fiber over the DUT and performs the XY sweep. The minimum achievable incremental movement corresponds to 50 nm and the bidirectional repeatability is 1.6 μm.

3 Comparison of Simulation and Experimental Results

To investigate the effect of the guard ring on the distribution of the electric field inside the SPAD, TCAD simulations are performed for both SPADs structures shown in Fig. 1. The structures are defined based on the SPADs' layouts and the process design kit information as well as the doping profiles (confidential data) provided by the foundry, and according to the cylindrically symmetric geometry of the SPADs, two-dimensional (2D) simulations are carried out along one diameter. The key parameters and the corresponding values used in the TCAD simulations are shown in Table 1.

Figure 3 shows the built-in electric field at an excess bias voltage of 6.6 V obtained by using the Geiger mode device simulation feature of SILVACO Atlas.[22] The 2D plots of the electric field distribution inside the two structures with the physical and virtual guard rings are shown in Figs. 3(a) and 3(b), respectively. Both SPADs show a similar electric filed profile (direction and strength) in the central area where the guard ring has no influence on the electric field. Therefore, in both structures, a vertical electric field [along the direction x as shown in Fig. 2(c)] is formed at the center of the device ($r = 0$) with a very high strength (700 kV/cm) at the interface of n^+/p-well (multiplication region) and a lower amplitude (8 kV/cm) over the depletion region (i.e., absorption region), which extends down to the substrate. As a result, when a photon is absorbed in the depletion region, the generated electron and the hole are promptly separated by the electric field (in opposite directions) and then, the minority carrier is accelerated toward the multiplication region.

Inside the multiplication zone, the strength of the electric field is significantly reduced when moving away from A toward the guard rings as is shown in Fig. 3(d). As a result, the avalanche multiplication region is limited to the junction of n^+/p-well where the electric field is very high and surrounded by the guard ring, and thus, the edge breakdown is avoided at the cost of a reduced active area. It can be seen from a lateral cross-section of the electric field through $A - A'$ ($x = 0.5$ μm), the high-electric field in SPAD1 starts falling down (at ~37 μm) earlier than in SPAD2 (at ~39 μm), which makes the multiplication region smaller. In addition, the r-component (i.e., the lateral component) of the electric field at the edge (i.e., the end of p-well)

Table 1 Key parameters used in the TCAD simulation performed by ATLAS.

Parameter	Discription	Value
An	Impact ionization constants for electron[21]	7.03×10^5 1/cm
En_crit		1.231×10^6 V/cm
Ap	Impact ionization constants for hole[21]	1.58×10^6 1/cm
Ep_crit		2.036×10^6 V/cm
taun	Electron life time	200 μs
taup	Hole life time	200 μs
L_e	Electron diffusion length	270 μm
L_h	Hole diffusion length	90 μm

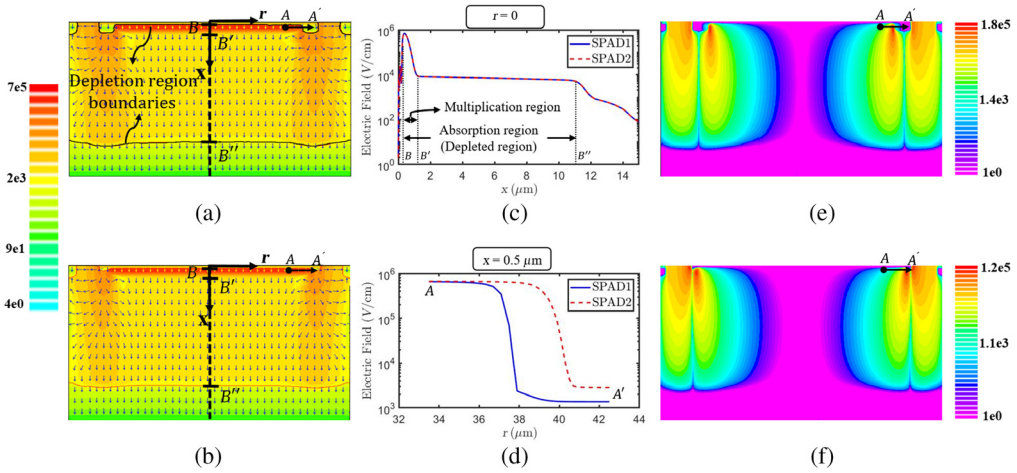

Fig. 3 2D plots of the electric field obtained by TCAD simulation for (a) SPAD1 and (b) SPAD2 in logarithmic scale. Arrows indicate the local electric field direction. (c) A vertical cross-section of the electric field at the center ($r = 0$) for both SPAD1 and SPAD2. (d) A lateral cross-section of the electric field through A–A' at $x = 0.5$ μm in SPAD1 and SPAD2. 2D plots of the r-component of the electric field for (e) SPAD1 and (f) SPAD2 in logarithmic scale.

grows due to the formation of a lateral p-well/n-well junction and a p-well/p-epi transition in SPAD1 and SPAD2, respectively, as shown in Figs. 3(e) and 3(f). As a result, the carriers photo-generated at the border of the active area [below A–A', see also Figs. 3(a) and 3(b)] are exposed to a non-vertical electric field, which deviates the generated minority carriers (i.e., the electrons) from their pure vertical trajectory toward the lower-electric field region (out of the multiplication region). Therefore, the active area covers a smaller area as compared to the area covered by the n^+/p-well junction in the layout and can be named as the effective active area in contrast to the physical active area defined by the layout dimensions.

To visualize the effective active area inside these structures, the avalanche triggering probability (ATP) is obtained by TCAD simulation. ATP is defined as the probability that either a photo-generated electron or a hole (as two independent events) at a position x initiates a self-sustaining avalanche event, depending on the impact ionization coefficients and the electric field. More details and how ATP leads to PDP are explained in our recent paper.[23] Figure 4 illustrates a 2D plot of the ATP for both structures. Here, in spite of the fact that the avalanche process happens only in the multiplication region, a carrier generated outside the multiplication region can reach this area and trigger an avalanche event. Therefore, the ATP corresponding to the avalanche triggering probability (for a self-sustaining avalanche) of the minority carries (i.e., electrons) below the multiplication zone extends to the p-well and p-epi regions and shows a maximum value (at the central region). In fact, it shows a fixed (maximum) value over this region ($r < 20.5$ μm and $r < 27.5$ μm, respectively) as we can assume a negligible recombination rate due to a strong drift toward the multiplication region. This means that an electron generated at any x ($r < 20.5$ μm and $r < 27.5$ μm, respectively) drifts toward the cathode and will flow through the whole multiplication region. Similarly, for the area above the multiplication region (n^+ layer), a minority carrier (i.e., a hole) can reach the multiplication region and trigger an avalanche event.

Figure 4 demonstrates that a larger effective active area is obtained with the virtual guard ring compared to the physical guard ring. The difference between the radii of the effective active areas in the two structures is larger than the ~2 to 3 μm predicted by Fig. 3(d) and is around 7 μm. This is due to the lateral electric field from the lateral diode (p-well/n-well) in SPAD1, which is stronger than that of the p-well/p-epi transition in SPAD2, and therefore, it has a stronger effect on the trajectory of the carriers toward the cathode and results in a narrower region with a high ATP. This proves an improvement of around 45% and accordingly, for the same diameter of 116 μm the fill-factors of 23% and 34% are obtained for SPAD1 and SPAD2 leading to the photon detection efficiencies (PDEs, PDE = PDP times fill-factor) of 7.75% and 11.46%, respectively.

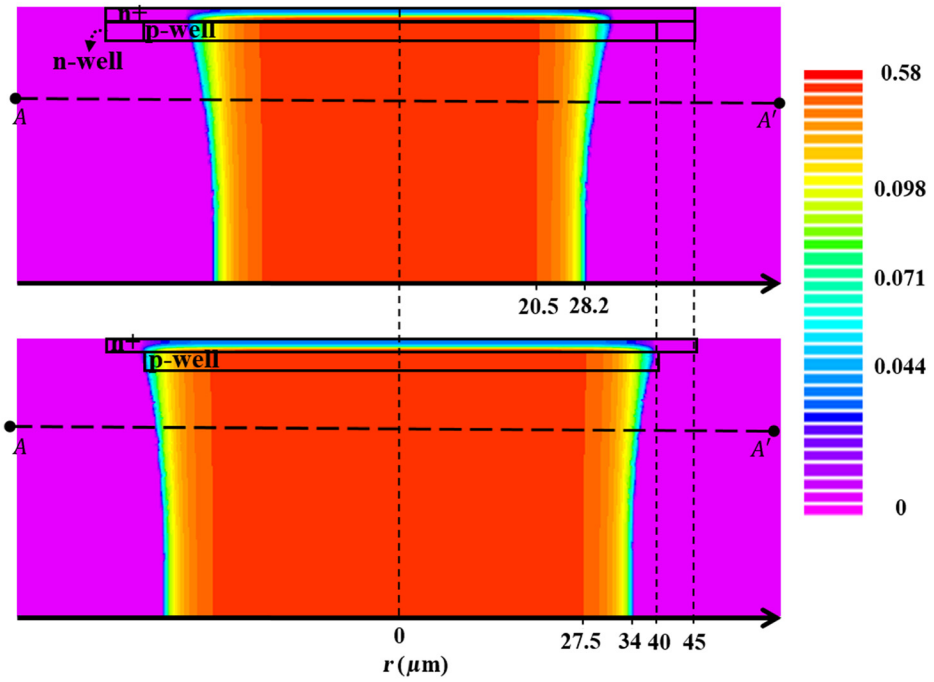

Fig. 4 2D plots of the ATP at an excess bias voltage of 6.6 V for (a) SPAD1 and (b) SPAD2.

To experimentally characterize the effective active area, the radial dependency of the PDP is measured at a wavelength of 635 nm. Figure 5(a) shows the measured PDPs for both structures as a function of the distance between the center of the SPAD and the center of the light source. Furthermore, ATPs (1D cross-section at $x = 5$ μm) obtained by simulation are added to this figure. It is worth mentioning that the ATP is independent of the wavelength; however, here we plot it for a cross-section depth equal to the penetration depth (σ) at $\lambda = 635$ nm. In fact, σ is a function of λ and defines the depth at which the optical power decays to $1/e$ of its value at the silicon surface. The result verifies the expected difference between the diameters of the effective active area of the two structures predicted by the simulation. Furthermore, the PDP curves show a smaller slope to zero as compared to the ATP curves because due to the actual beam widths the PDP is averaged over the light spot on the SPAD.

Figure 5(b) shows the reverse current in dependence on reverse voltage [i.e., the $I(V)$ curves] for SPAD1 and SPAD2. As it is shown, the breakdown voltage of SPAD1 is lower than that of SPAD2, which originates from the difference in the electric field distribution in the two SPADs. Table 2 shows a comparison of the parasitic noises at an excess bias of 6.6 V and of the breakdown voltages of SPAD1 and SPAD2. The breakdown voltage is read as the reverse voltage for a

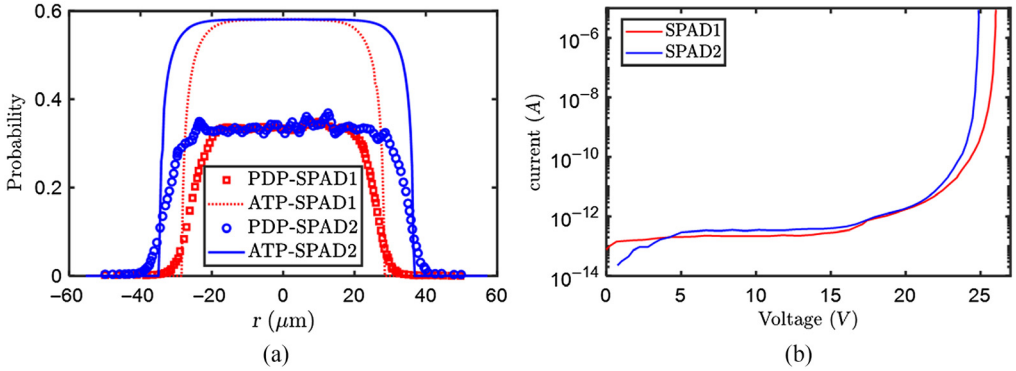

Fig. 5 (a) Measured radial PDPs and simulated 1D cross-sections of the ATP at an excess bias voltage of 6.6 V. (b) Measured $I(V)$ curves.

Table 2 Parasitic noise, breakdown voltage, and the PDE comparison of SPAD1 and SPAD2 at an excess bias of 6.6 V.

SPADs	DCR	APP	V_{br}	PDE
SPAD1	30.43 kcps	4.25%	25.8 V	7.75%
SPAD2	31.14 kcps	5.29%	24.9 V	11.46%

reverse current of 10 μA. It can be seen that the DCR and APP of SPAD2 are slightly higher than that of SPAD1, which is due to the fact that SPAD2 has a larger effective active area compared to SPAD1. Therefore, one can say that employing the virtual guard ring in this structure is efficient to improve the fill-factor while retaining its efficiency from the other performance factors point of view.

4 SPAD Scalability with the Virtual Guard Ring

Maintaining the overall sensitivity and providing an acceptable fill-factor is a challenge when the SPAD is scaled-down. Therefore, the fill-factor enhancement using the virtual guard ring becomes more significant in smaller SPADs. Here, we study the effect of the guard ring on the fill-factor of a SPAD with a diameter of 48 μm and the n^+ diameter of 30 μm. To achieve a higher fill-factor, the width of the virtual guard ring has to be minimized that the fill-factor is maximized but still the edge breakdown is not happening. According to the design rules and the doping profiles associated with the 0.35-μm CMOS technology, we have obtained a minimum width of around 1 μm for the virtual guard ring using TCAD simulations. In fact, if the width of the virtual guard ring (i.e., the radius of the n^+ minus the radius of the p-well) is smaller than 1 μm, the electric filed at the edges will be higher than in the center and as a result, the breakdown occurs at the edge area at a smaller reverse bias voltage and only the edge area of the diode will contribute to the SPAD operation in Geiger mode. Figure 6 shows this effect for a virtual guard ring of 0.5 μm where the active area is limited to the edges.

Now, we compare the smaller SPAD (device diameter = 48 μm, n^+ diameter = 30 μm) with the physical guard ring (p-well diameter = 20 μm, n-well width = 5 μm) to the SPAD with the minimized virtual guard ring (p-well diameter = 28 μm, guard ring width = 1 μm), using TCAD simulations as shown in Fig. 7. It can be seen that the effective active area of the SPAD with the physical guard ring is severely degraded and shows a fill-factor of less than 1%, which is not suitable for practical applications. On the other hand, the SPAD with the virtual guard ring retains its efficiency and provides a much higher fill-factor of around 22% (the radius of the effective active area is 11.3 μm at the cross section of A–A') leading to a PDE of 7.5%, which can be acceptable for many applications. According to these results, only the SPAD structure with a diameter of 48 μm and the virtual guard ring of 1 μm was fabricated in 0.35-μm OPTO-ASIC CMOS technology. This SPAD was characterized through a similar experiment as it was explained above. Its measured radial PDP at a wavelength of 770 nm and its measured

Fig. 6 2D plot of the ATP for the SPAD with a 0.5-μm virtual guard ring.

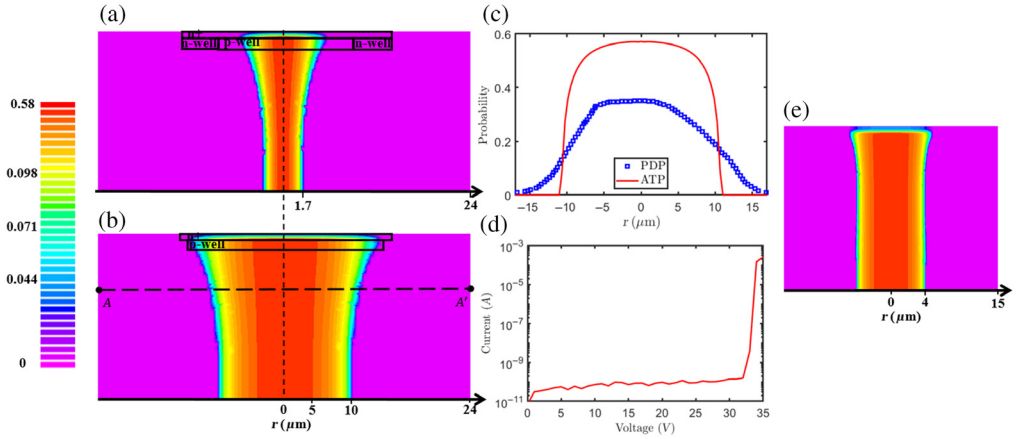

Fig. 7 2D plots of the ATP for the SPADs with a diameter of 48 μm and (a) the physical guard ring, (b) the virtual guard ring at an excess bias voltage of 6.6 V. (c) The measured radial PDP and a 1D cross-section of the ATP of the SPAD with the virtual guard ring at the depth of 5 μm and at an excess bias voltage of 6.6 V. (d) Measured $I(V)$ curve of the SPAD with the virtual guard ring. (e) A 2D plot of the ATP for a 1-μm-virtual-guard-ring SPAD with a diameter of 30 μm (n^+ diameter = 15 μm).

$I(V)$ curve are shown in Figs. 7(c) and 7(d), respectively. This SPAD is from a different process run and its breakdown voltage cannot be compared to those of SPAD1 and SPAD2. For this SPAD at an excess bias of 6.6 V, DCR and APP are 7.5 kcps and 14.2%, respectively. Figure 7(c) shows a comparison of the measured radial PDP and the simulated profile of the ATP at a depth of 5 μm [over A–A' as shown in Fig. 7(b)]. As it is mentioned above, the PDP curve decreases with a smaller slope compared to the ATP curve due to the fact that the measured PDP at each point is an average over the light spot on the SPAD. Here, a single-mode fiber with a core diameter of 8 μm was used for scanning the SPAD, which shows a larger difference between PDP and ATP compared to the result in Fig. 5(a).

To further investigate the scalability of the SPAD structure with virtual guard ring in the available 0.35-μm CMOS technology, we obtain the ATP for a structure with a diameter of 30 μm using TCAD simulations as is shown in Fig. 7(e). This result suggests that, at this size, it is possible to achieve a fill-factor of around 7%, which is not appropriate for application where high sensitivity is critical, e.g., optical receivers based on an array of a few SPADs. However, one may still consider this as an acceptable fill-factor for other applications, where large arrays consisting of hundreds or thousands of SPADs are used and the fill-factor is more critical. Table 3 shows a comparison of the key performance parameters of the SPAD in this work with those of previously published SPADs to better highlight the contribution of this work over the state of the art.

Table 3 Performance comparison of the implemented SPAD with literature.

SPADs	PDP at $\lambda = 635$ nm	DCR (cps/μm^2)	Diameter	Fabrication process
Ref. 15	7.2% at $V_{ex} = 2$ V	73 at $V_{ex} = 2$ V	4 μm	CMOS 65 nm
Ref. 16	10% at $V_{ex} = 3$ V	4.7 at $V_{ex} = 3$ V	30 μm	CMOS 180 nm
Ref. 19	9% at $V_{ex} = 5$ V	8.8 at $V_{ex} = 5$ V	15 μm	—
Ref. 24	15% at $V_{ex} = 4$ V	16 at $V_{ex} = 4$ V	12 μm	CMOS 180 nm
Ref. 25	15% at $V_{ex} = 4$ V	2 at $V_{ex} = 4$ V	20.4 μm	CMOS 180 nm
Ref. 26	7% at $V_{ex} = 11$ V	1.5 at $V_{ex} = 11$ V	—	CMOS 180 nm
This work	35% at $V_{ex} = 6.6$ V	3.2 at $V_{ex} = 6.6$ V	48 μm	CMOS 350 nm

To compare the performance of different SPADs, one should consider many parameters including the technology in which the SPAD is implemented, the size of the SPAD, and the measurement conditions. Nevertheless, as the SPAD presented in this paper is designed to be used for optical fiber receiver applications, its PDP is significantly larger than that of the other published results. To have an understandable DCR comparison, we should normalize the DCR by the SPADs' area. It is shown that the DCR/μm^2 of the presented SPAD is comparable with the other published results. Table 3 also includes the diameter of the SPADs to provide an insight into the size of the SPADs reported in literature. It is worth noting that the availability of doping profiles and the design rule limitations of the fabrication process play a key role in the scalability of SPADs. It is clear that advanced, smaller-node technologies offer higher scalability features. In addition, in technologies where higher doping concentrations are available, smaller structures can be fabricated. However, comparison of the scalability of different technologies is out of the scope of this work. According to our result, in the same technology using the same doping profiles, replacing the physical guard ring by the virtual guard ring can improve the effective fill-factor of the SPAD.

5 Conclusion

The use of a virtual guard ring is a practical solution to avoid the edge breakdown effect in SPAD devices and still preserve the fill-factor as an important performance metric. An experimental and simulation study on the effect of the virtual guard ring on the fill-factor and the scalability of a n+/p-well SPAD implemented in 0.35-μm CMOS technology is presented. A minimum guard ring width of 1 μm is obtained using TCAD simulation and is used to design smaller SPADs in this CMOS technology. A fill-factor of around 22% is achieved for a SPAD with a diameter of 48 μm, and it is shown that the fill-factor decreases to below 7% for a SPAD with the diameter less than 30 μm. We believe that higher fill-factors at smaller SPAD sizes are achievable only in more advanced CMOS technologies where doping concentrations are higher.

Acknowledgments

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