CMOS MEMS Technology and CAD: the Case of Thermal Microtransducers

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ABSTRACT

Thermally-based transducer microsystems can be made by using CMOS IC technology, post-CMOS micromachining or deposition, and flip-chip packaging. Technology steps, materials, and physical effects pertinent to thermal microtransducers are summarized together with microheater, thermistor, thermopile, thermal isolation, and heat sink structures. An infrared intrusion detector, a thermal air flow sensor, and thermally excited microresonators for acoustic and chemical sensing serve as demonstrators. We discuss the characterization of process-dependent properties of CMOS materials crucial for thermal microtransducer CAD.

Keywords: CMOS microsensor, micromachining, thermal sensor, infrared sensor, flow sensor, position sensor, chemical sensor, thermal CMOS material properties.

1. INTRODUCTION

Direct thermal sensors convert temperature or heat to electrical signals. Indirect thermal sensors convert radiation, electrical power, or the presence of chemical species via thermal effects to the final electrical output signal. Other indirect thermal sensors are based on thermal actuation effects such as resistive heating and thermal expansion. These effects can be exploited for flow, pressure, position or chemical sensors.

Thermal microsensors based on CMOS technology became feasible when CMOS compatible micromachining was established. Micromachining allows to remove thermally conducting materials (in particular the highly conducting bulk silicon) for thermal isolation of heated microstructures. Merging CMOS IC technology with micromachining allows to provide sensors with on-chip bias and signal conditioning circuits. On-chip circuits are crucial to pick up small signals such as the thermoelectric voltage in the μV range of CMOS infrared intrusion detectors.[1] The small size and low power consumption of CMOS microsensors allows battery-operated pocket-size instruments such as an air flow velocity meter of the size of a ballpoint pen.[2]

Post-CMOS micromachining processes include wet and dry etching for bulk and surface-micromachining, applied from the front or the back of the finished CMOS wafer, with KOH or EDP etchants. Such processes allow to produce dielectric membranes with sandwiched polysilicon and metal structures for heaters and thermopiles[3] or thermally excited silicon membranes for ultrasound (up to 100 kHz) transducers.[4,5]

This keynote updates or complements previous overviews.[6,7,8] A comprehensive review article on micromachined thermal microtransducers is forthcoming.[9]

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2. TECHNOLOGY SUMMARY

Thermally-based microtransducers can be made by combining industrial CMOS IC technology with additional compatible processing steps, e.g., anisotropic etching of silicon or thin film deposition of "non-IC" materials. Preferably, they are performed as "post-processing" or "post-CMOS" steps, i.e., after completion of the regular IC process sequence. The additional processing must be compatible with the foregoing IC process. To this end the maximal temperature is limited to about 400 °C in order to preserve the aluminum structures of the preceding IC process. Many standard micromachining steps, such as anisotropic etching of silicon or sacrificial layer techniques, have been demonstrated to be indeed compatible with industrial IC processes.

The variety of micromachined silicon transducers can be divided in two major categories: bulk-micromachined transducers (Figs. 1(a)-(d)) made by machining of the silicon substrate and surface-micromachined transducers (Figs. 1(e) and (f)) built from stacked thin films. Obviously, bulk-micromachining and surface-micromachining techniques can be combined. In the case of thermal sensors, micromachining is usually employed to thermally isolate the sensor structure or part of it from the bulk silicon. This can be done by bulk-micromachining, either from the front or the back of the wafer, as well as by surface-micromachining. Fig. 1 illustrates six possible post-CMOS etching techniques.

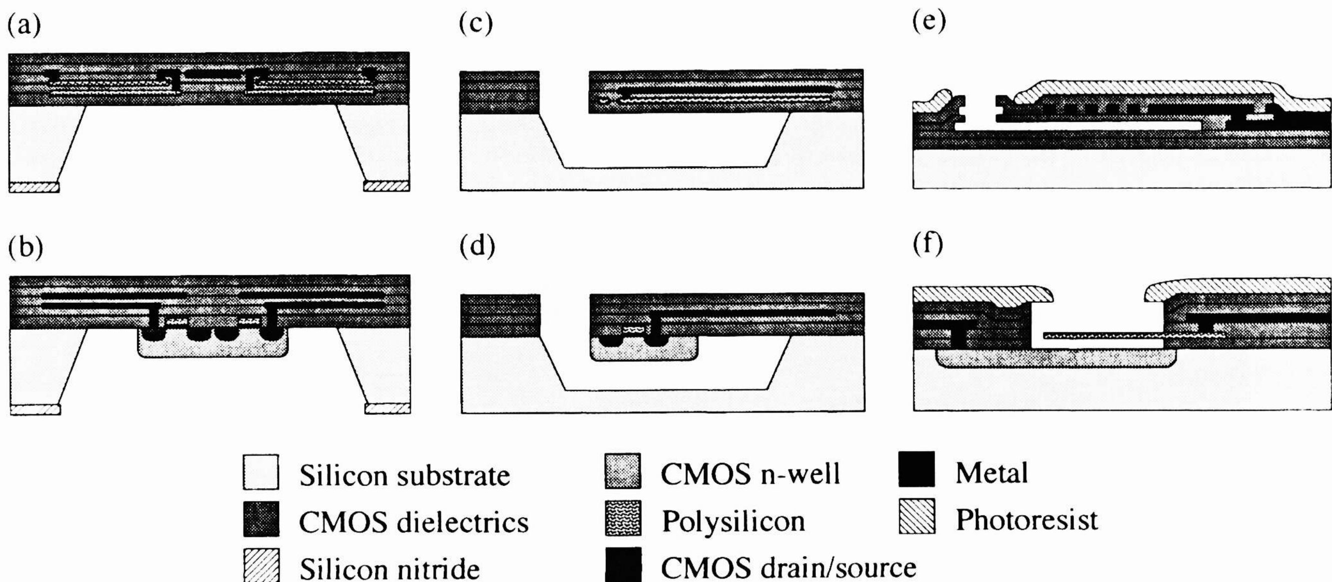

Figure 1: Schematics of six post-CMOS micromachining techniques: rear bulk-micromachining (a) without and (b) with electrochemical etch stop on CMOS n-well; front bulk-micromachining (c) without and (d) with electrochemical etch stop; surface-micromachining based on (e) sacrificial aluminum and (f) sacrificial silicon oxide etching.

Rear bulk-micromachining, i.e., anisotropic etching from the back of the wafer (Figs. 1(a) and (b)), serves to release membrane structures. The anisotropic etching step from the rear of the wafer is usually performed in a potassium hydroxide (KOH) solution.[1,10] The wafer front is typically protected from the etching solution by mechanical housing. An additional polymer layer on top of the CMOS passivation can be used to prevent accidental KOH breakthrough and, therefore, to increase the reliability of the micromachining process.[11] The rear side of the fully processed wafers has to be prepared for the wet etching step. In order to ensure good etching results, a planar and defect free silicon surface must be achieved. The required surface quality can be obtained by chemical-mechanical polishing or using a spin etcher.[3,11] A silicon nitride or silicon oxide layer is deposited and patterned on the wafer back to define the etch windows.

Membrane structures consisting of the dielectric layers provided by the CMOS process are obtained by etching through the complete silicon wafer (see Fig. 1(a)). The thermal oxide acts as etch stop. Dielectric membrane structures are used for sen-

sors requiring thermal isolation, such as thermal radiation and flow sensors. The stress in the thin dielectric membranes limits their mechanical reliability. Typically, the thermal oxide is under compressive stress of about 300 MPa. The overall stress within the dielectric sandwich can be controlled by adjusting the intrinsic stress of the passivation layer.

Silicon membranes as well as complex suspended n-well structures are obtained by combining the anisotropic etching step with an electrochemical etch stop technique.[10,11] The etching stops at the pn-junction between CMOS n-well and p-type substrate. During the electrochemical etching step, etching potentials have to be applied to the structural n-wells and the substrate. This technique provides microstructures with the excellent mechanical properties inherent in silicon. Active devices can be designed within such silicon structures. The technique is available as foundry service by *AMS Austria Mikro Systeme, Austria*.

Front bulk-micromachining (Figs. 1(c) and (d)) is used to release cantilever beams, bridges and suspended membranes. Typically, the anisotropic etching is either performed in an ethylenediamine/pyrocatechol (EDP) or a tetramethylammonium hydroxide (TMAH) solution. Compared to KOH, these solutions usually offer lower silicon etch rates in <100> direction, but increased selectivity with respect to aluminum and silicon dioxide. By overlapping an active area, a contact opening, a via, and a pad opening in the sensor design, parts of the silicon substrate are exposed to the ambient and can be attacked by the etchant. Otherwise, the dielectric layers serve as "natural" etch mask. Due to the anisotropic etching characteristics, convex corners in the design are underetched and microstructures, such as cantilever beams, are released.

As an example, Fig. 2 shows a test structure for measuring the heat capacitance of the thin film materials involved in the CMOS process. The structure consists of the CMOS dielectric layers. Sandwiched in-between are polysilicon heating resistors and a metal layer. The metal pads shown in Fig. 2 are covered with gold bumps. These gold bumps are electroplated routinely on the metal pads of the CMOS processes of *EM Microelectronic Marin, Switzerland* to prepare the dice for tape-automated-bonding. Gold bumps can serve as thermal mass to increase thermal time constants[3] or reduce thermal cross-talk.

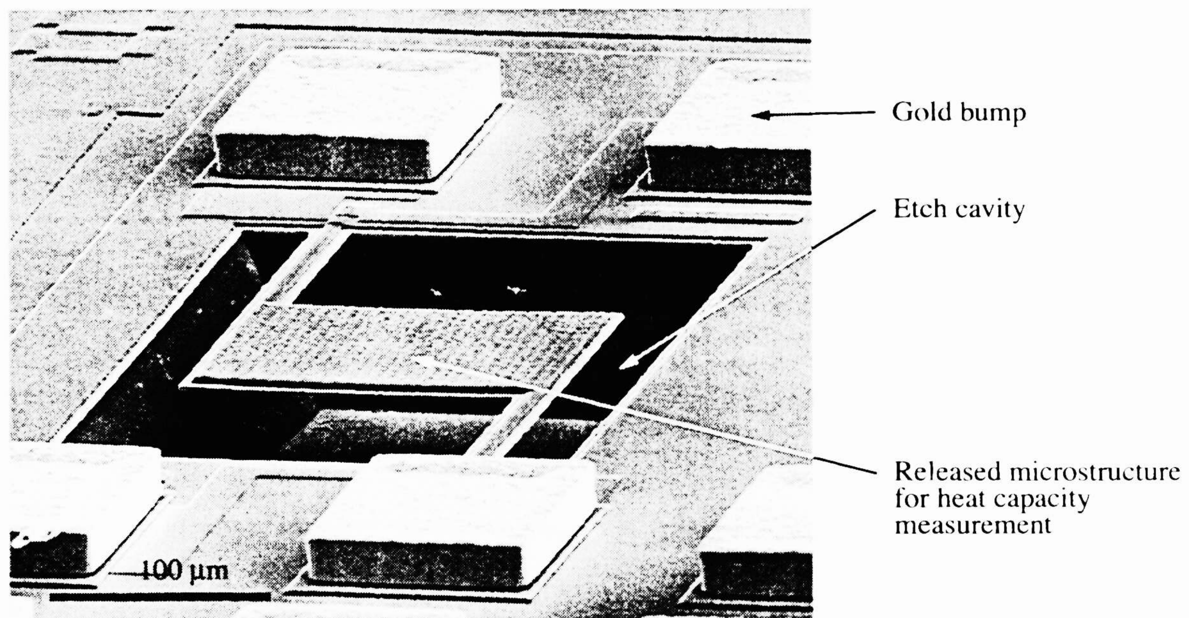

Figure 2: SEM micrograph of microstructure to measure the heat capacitance of CMOS thin films; the device was released by a maskless front bulk-micromachining step using EDP.[12]

Surface-micromachining generates mechanical structures from stacked thin films. The basic technology is the sacrificial layer technique: a mechanical structure is released by removing a layer underneath it (Fig. 1(e) and (f)). Common sacrificial layer materials used with CMOS transducers are silicon dioxide and aluminum.

Thin-film deposition can be applied as a further type of post-processing step. Examples are the CMOS-compatible deposition of chemically sensitive layers, such as polymers, for chemical sensors, or the deposition of soft magnetic Ni-Fe films for improved sensitivity of magnetic sensors.

3. BASIC MATERIALS, EFFECTS, AND COMPONENTS

Sensors require physical or physico-chemical transduction effects, materials exhibiting such effects, and structures which isolate the transduction effects. For example, thermocouples need the Seebeck effect, conducting materials with sufficiently large Seebeck coefficient, and thermally isolated, electrically connected legs. Narrowed down to CMOS thermal microsensors, this means that we must use the materials provided by the CMOS IC process, exploit the thermal (and coupling) effects inherent in the CMOS materials, and design structures which bring out the transducer effects, within the limits of the CMOS and post-CMOS fabrication rules.

CMOS materials include bulk silicon, polysilicon (possibly both n- and p-doped), dielectrics (silicon oxide, silicon nitride, passivation) and metal (alloy with mainly aluminum). In addition, epitaxial silicon is available in the case of BiCMOS technology. All these materials can serve as thermal mass. Silicon and metal conduct heat efficiently. The dielectric layers provide only moderate thermal isolation in view of their small thicknesses. That is why removal of material by micromachining is required for efficient thermal isolation.

The thermoresistive effect (Joule heat) allows to use the electrically conducting materials (notably polysilicon) for resistive heating. The temperature coefficient of resistivity, notably that of polysilicon, is exploited for resistive thermometers (thermistors). The difference in thermopower (Seebeck coefficient) between different conducting CMOS materials (including differently doped silicon areas) is the basis of integrated thermocouples and thermopiles. The different thermal expansion coefficients of different CMOS materials produce the bimorph effect, which is exploited for the thermomechanical actuation of micromechanical structures.

The thermal properties of silicon depend on doping and crystalline structure. For example, the temperature coefficient of the resistivity of polysilicon can be positive or negative, depending on doping. All material properties are temperature dependent. The material properties are process-dependent and have to be known before an optimized thermal sensor can be designed for fabrication by a specific CMOS process. Table 1 provides examples of such data, namely the resistivities, the temperature coefficients of resistivity, the Seebeck coefficients, and the thermal conductivities, of different polysilicon layers, from different CMOS IC processes and suppliers.[6]

Table 1: Measured material properties of a 1.2 μm CMOS process of AMS, a 2 μm CMOS process of EM, and a 1 μm CMOS process of ATMEL ES2; sheet resistance ρ_{sq}, temperature coefficient (TC) of ρ, majority carrier density n(p), Seebeck coefficient α, and thermal conductivity κ, with error estimates.[6]

	$\rho_{sq} \pm 2$ % [mΩ/cm]	TC of ρ [10^{-3} K^{-1}]	n(p) ± 7 % [10^{20} cm^{-3}]	$\alpha \pm 5$ % [μV/K]	$\kappa \pm 2.5$ [W/(m·K)]
AMS					
Gate-poly (n^+)	25	0.86	3.4	-120	28
Capacitor-poly (p^+)	215	-0.14	1.6	190	19
EM					
Gate-poly (n^+)	32	0.89	2.04	-108	19
Gate-poly (n)	2600	-4.40	0.04	-520	22
E2PROM-poly (n^+)	27	0.83	1.75	-111	17
Gate-poly (p^+)	425	0.59	0.33	330	20
ES2					
Gate-poly (n^+)	31	0.54	1.27	-108	16
Gate-poly (n^+)	45	0.49	0.93	-128	24

CMOS resistors made of diffused silicon, deposited polysilicon, or metal lines can provide heating elements, thermistors, and strain gauges. The latter, while not being thermal devices in themselves, can be used to detect the thermal actuation of mechanical microstructures through the piezoresistive effect. For example, gate polysilicon heating resistors, several microns wide and several hundred microns long, are placed close to the hot contacts of a thermopile in thermoelectric gas flow sensors[2] and thermal converters[3], as shown in Fig. 3. Their resistance is typically 1 to 2 kΩ and their temperature coefficient is of the order of 850 ppm/K.

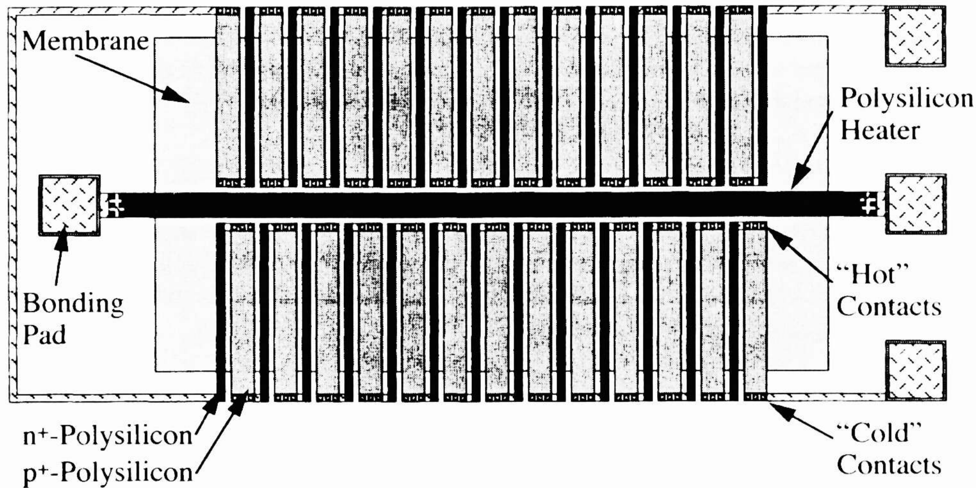

Figure 3: Design layout of a CMOS thermal converter on a dielectric membrane: the unknown ac voltage is applied to the center polysilicon heater; an n^+/p^+ polysilicon thermopile measures the resulting temperature elevation.[3]

CMOS thermocouples can be made of CMOS metal, polysilicon, and diffused bulk silicon. Metal/polysilicon and n-polysilicon/p-polysilicon thermocouples can be sandwiched between the CMOS dielectric layers and thermally isolated by removing the bulk silicon. Thermopowers as high as several hundred μV/K can be achieved. The n^+-polysilicon/p^+-polysilicon combination is preferable.[2,3] CMOS thermopiles typically consist of 5 to 100 thermocouples embedded in dielectric membranes with internal resistance of kΩ to MΩ and thermal conductance of the order of 0.1 mW/K. Thermopowers and sensitivities up to about 10 mV/K and 100 V/W, respectively, are achievable. A typical design is shown in Fig. 3.

Thermal isolation of the microsensors from all sources or sinks of heat other than those pertaining to the measurand are required. Thermal isolation is strongly improved by removing bulk silicon and embedding thermal microsensors in dielectric cantilever beams, bridges, or membranes. Thereafter, polysilicon or metal lines remain as vehicles of heat transfer as well as the surrounding air. Heat sinks and thermal uniformization require high thermal conductance. This can be provided by metal, bulk silicon, and polysilicon. The silicon substrate usually serves as keeper of the ambient reference temperature.

4. THERMAL RADIATION SENSOR

In thermal infrared (IR) sensors, incoming radiation is absorbed and converted to heat, and the resulting temperature increase is converted to an electrical output signal. In CMOS-based IR detectors, conversion is performed with integrated polysilicon/metal or bidoped polysilicon thermopiles or with integrated thermistors (bolometers). A prerequisite for maximum responsivity is the efficient thermal isolation of the absorber. Surface-micromachined plate structures and bulk-micromachined bridges or membranes composed of thin film dielectrics have been proposed to provide appropriate supporting structures.

CMOS compatible thermoelectric infrared arrays have been fabricated using a commercial 1 μm single-poly double-metal CMOS process.[1] Membranes composed of the standard CMOS dielectrics with stress-compensating passivation contain the two-dimensional arrays of IR pixels, with a pitch of 320 μm. Polysilicon/aluminum thermopiles are sandwiched between the dielectrics. The fabrication relies on rear bulk-micromachining. Thermal isolation of the pixels and mechanical stabilization

of the membrane are achieved by gold lines with a height and width of 25 μm, which are electroplated onto the CMOS dice. This allows industrial fabrication of membranes with size up 14 mm by 16 mm. The pixels have responsivities of 4.1 V/W and time constants below 10 ms. Pixel-to-pixel cross-talk is below 2000 ppm.

A multiplexer and amplifier system consisting of an input and output modulator, a fully differential chopper preamplifier, a bandpass filter, and a third gain stage are cointegrated with the arrays. The preamplifier achieves an exceptionally low noise power density of 15 nV/√Hz, 1.5 μV offset, and a common mode rejection ratio of 70 dB.[13] The thermopile resistance of 2 kΩ is matched to the amplifier characteristics. The component qualities allow to achieve an overall noise-equivalent power of the detector/amplifier system of 39 nW per pixel for a bandwidth of 100 Hz. No vacuum package is required for this performance. An example of a CMOS IR detector array microsystem is shown in Fig. 4.

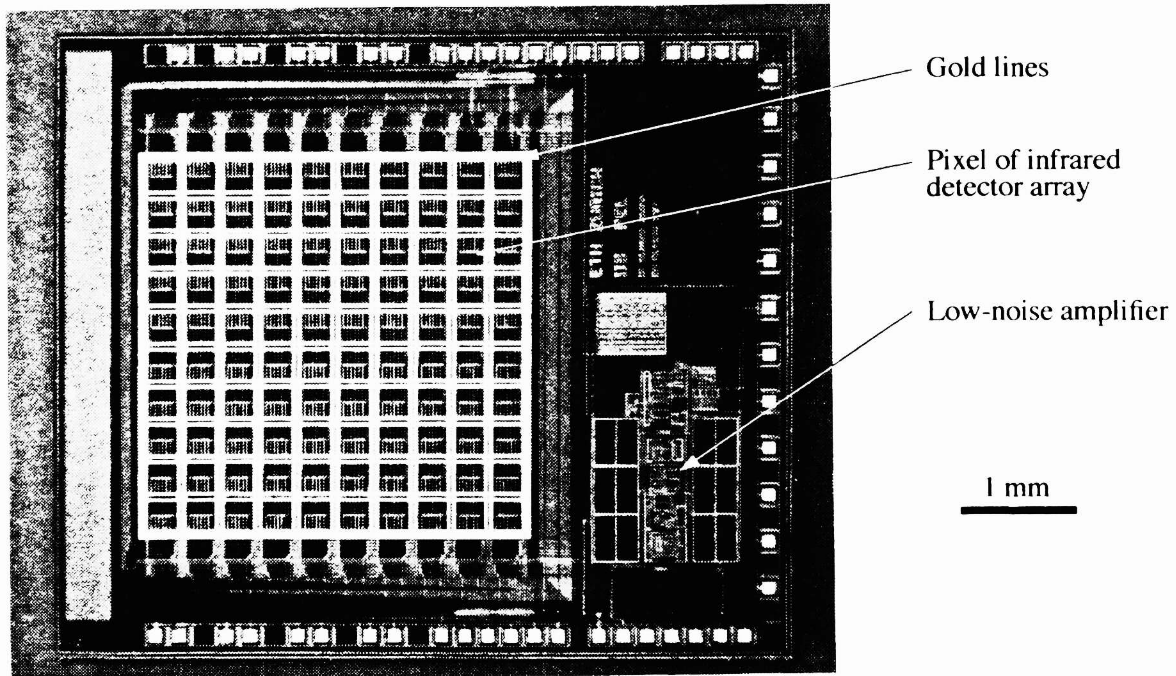

Figure 4: Photograph of rear bulk-micromachined CMOS IR detector array microsystem with on-chip amplifier system fabricated in the 1 μm CMOS process of EM; 10 by 10 pixels are located on a dielectric membrane stiffened by electroplated gold lines; overall chip dimensions are 6.3 mm by 5.4 mm.[1]

5. SENSORS USING THERMAL ACTUATION

Thermal flow sensors measure the convective heat transport by a fluid. The measurement is usually performed by thermally isolated structures such as cantilevers, bridges, or membranes containing heaters and temperature sensors. Heaters can consist of metal or polysilicon. Temperatures are monitored by metal or polysilicon thermistors, polysilicon/metal, or n-polysilicon/p-polysilicon thermopiles, or integrated diodes. Convective cooling is measured by miniaturized versions of the classical hot wire anemometer. In these structures the power needed to maintain a temperature difference between heater and the incoming gas flow is monitored. Another type of devices exploit flow-induced thermal asymmetries. At a fixed heating power, a velocity-dependent temperature difference is measured between downstream and upstream locations on a centrally heated structure. A recent flow sensor microsystem chip[2] combining a membrane sensor with on-chip power management and signal amplification and conversion circuitry, with rectangular electroplated gold frame and bumps for flip-chip mounting, is shown in Fig. 5 and further discussed in Section 7.

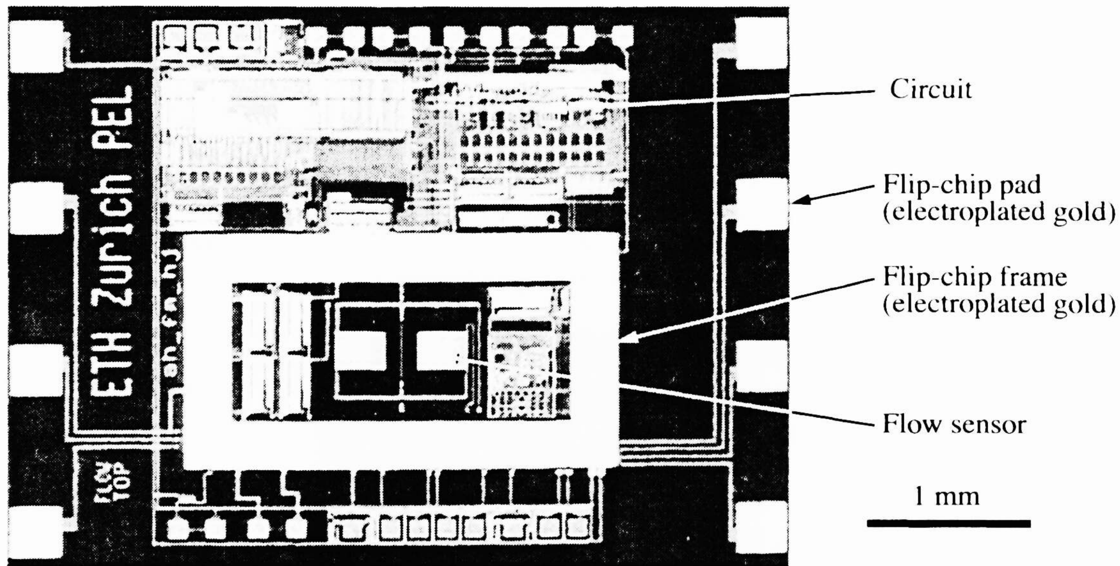

Figure 5: Microphotograph of CMOS chip with integrated thermoelectric flow sensor and on-chip circuit including two amplifier stages, A/D converter, and power management. The rectangular frame and bumps consist of electroplated gold and are used for the flip-chip packaging of the device.[2]

Thermomechanical actuation is a widely used driving mechanism for silicon based resonant structures and often combined with piezoresistive detection of vibrations. The required polysilicon or monocrystalline silicon resistors are standard components of industrial IC processes. As an example of a thermally excited resonant sensor, we mention the ultrasound barrier microsystem.[5] It consists of an ultrasound transmitting and receiving element facing each other at distances up to 150 mm. The ultrasound transmitter is operated at its fundamental resonance frequency and continuously generates ultrasound which is detected by the receiver unless the object to be detected interrupts the sound path. Micromachined membrane resonators are employed as ultrasound generating and receiving elements. The membranes are released in a post-processing anisotropic etching step with electrochemical etch-stop technique. The resulting membranes consist of monocrystalline silicon covered with the dielectric layers provided by the silicon process. Diffused resistors in the membrane center and close to the membrane edges are used as excitation and detection elements, respectively. Transverse membrane vibrations are generated by applying an ac voltage superimposed on a dc voltage to the driving resistor. With amplifying feedback-loop, the transmitting membrane is always operated at its fundamental resonance frequency of about 70-90 kHz. With an average heating power of 100 mW, typical vibration amplitudes and sound pressure amplitudes of 300 to 400 nm and 0.25 Pa (at 50 mm distance), respectively, are obtained at the resonance.

Thermally-based chemical sensors can be thermally actuated resonators whose resonance frequency is modulated by a change of mass due to absorption or desorption of chemical species. To this end, a chemically sensitive layer, e. g., a specific polymer, is deposited onto a CMOS cantilever beam.[14] The layer absorbs an amount of the analyte proportional to its concentration in the gas phase. Additional heating resistors under the polymer layer can be used to enhance desorption of the analyte or provide temperature dependent detection to improve selectivity. Another type of thermal chemical sensors uses a sensitive layer deposited on a thermopile or thermistor which detect temperature modulation due to enthalpy changes.

6. THERMAL CHARACTERIZATION OF CMOS MATERIALS

Besides geometrical data, reliable values of thermophysical material properties are essential for the simulation of thermal CMOS microsystems.[15] Properties of interest include the temperature-dependent sheet resistance of CMOS conductors, the thermal conductivity of individual CMOS thin films, dielectrics and conductors, the thermopower of semiconducting layers against metallization, and the heat capacity of the layers. Sheet resistances are routinely measured by the van-der-Pauw

method. Measurement of the other three classes of properties involve dedicated test microstructures fabricated in CMOS technology followed by compatible front bulk-micromachining.

The **thermal conductivity** of CMOS thin films is determined by microstructures of the type shown in Fig. 6. The structures are composed of a broad main cantilever with narrow lateral arms, suspended over a micromachined cavity. The cantilever consists of various sandwiches of the CMOS layers, including dielectric films, polysilicon layers, and/or metallizations. By appropriate layout design, two gate polysilicon resistors are integrated into their free end. One resistor is used as a heater, while the other serves as a thermistor. An integrated rectangular cover sheet made of the CMOS metals homogenizes the temperature distribution over the two polysilicon structures. When power is dissipated in the heater, the temperature of the cantilever tip increases. In order to determine the thermal conductivities of individual thin films, the composition of such cantilevers is systematically varied. The comparison of structures differing by a single layer allows to extract the conductivities from measurements of dissipated power per temperature increase. For a double-poly, double-metal CMOS process with field oxide, contact oxide, intermetal dielectric, and passivation layer, a minimum of nine structures is required.[16]

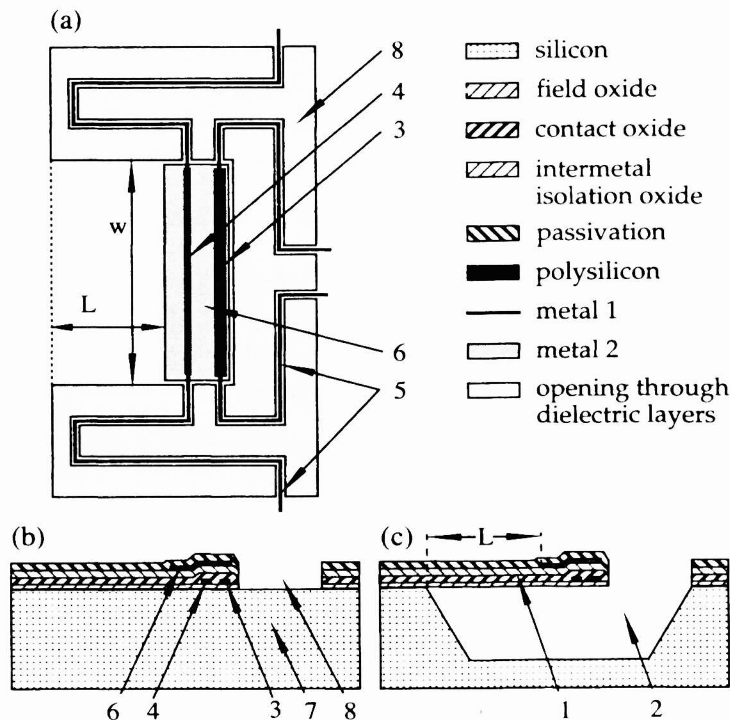

Figure 6: Schematic top view (a) and cross-sections (b,c) of microstructure to determine thermal conductivities of CMOS thin film sandwiches.[16] *Cross-section (b) after CMOS process and (c) after post-processing. 1: cantilever, 2: etched cavity, 3: polysilicon heater, 4: polysilicon temperature monitor, 5: metal connections, 6: metal cover for temperature homogenization, 7: silicon substrate, 8: openings through CMOS dielectrics; typical beam length* $L = 100\ \mu m$.

Using this method, it was found that thermally grown oxides have a thermal conductivity κ between 1.08 and 1.28 W/(m·K). The κ of deposited thin oxide films varies between 0.91 and 1.65 W/(m·K). Between 120 and 420 K the temperature-dependent κ values of various silicon oxides generally lie within -35% and +15% of the recommended value for fused bulk silica. CMOS gate and capacitor polysilicon layers have thermal conductivities between 17.2 and 32.6 W/(m·K) at 300 K, with TC between -1100 and 0 ppm/K, whereas κ of pure silicon is 156 W/(m·K). Aluminum-based CMOS metallizations investigated so far have shown thermal conductivities between 173 and 238 W/(m·K). These values are correlated with the electrical conductivity σ of the layers, and agree within 10% with the predictions of the Wiedemann-Franz law.

The **Seebeck coefficient** of semiconductor materials can be measured using a thermocouple. A semiconductor sample is contacted at two ends; one end is heated, while the other is coupled to a heat sink. Contact temperatures are monitored and the thermoelectric voltage between the contacts is measured. The Seebeck coefficient of standard CMOS polysilicon layers against CMOS metal layers has been measured with polysilicon/aluminum thermocouples. These are integrated into front bulk-micromachined cantilevers made of the full sandwich of dielectric CMOS layers. At their free end, the structures contain a heater and a thermistor for the measurement of temperature changes. Both are made of CMOS gate polysilicon. Heating powers of 125 μW establish temperature differences of roughly 10 K. For example, the n-doped gate and capacitor polysilicon layers of the double-poly double-metal 1.2 μm CMOS process of AMS show room-temperature Seebeck coefficients of -107±1.5 μV/K and -95.7±0.6 μV/K, respectively. Generally, the thermopower of the gate polysilicon of commercial ASIC processes ranges between -89 and -120 μV/K. These layers are typically n-doped in the lower 10^{20} cm^{-3} range and have a TC of α of about $3 \cdot 10^{-3}$ K^{-1} at room temperature.[6]

The **heat capacities** of the individual CMOS thin films affect the transient behavior of CMOS transducers. Accurate calorimetric measurements are required to determine these heat capacities. An example of a CMOS microcalorimeter devised to this end is the suspended plate structure with meandering polysilicon heater/thermistor[16] shown in Fig. 2. Heat dissipation by an AC current establishes a time-dependent temperature profile with a component at the second harmonic angular frequency. In this way, an average volumetric heat capacity of 1.66±0.06 MJ/($m^3 \cdot K$) was determined for a typical CMOS microtransducer sandwich composed of all dielectrics, polysilicon, and one metal layer. In the same units, the corresponding figure for a commercial CMOS passivation is 1.82±0.12, for the stack of CMOS dielectrics 1.74±0.13, and for CMOS metallizations between 2.45±0.21 and 2.81±0.34.

7. PACKAGED THERMOELECTRIC AIR FLOW SENSOR

The microsystem die of Fig. 5 is flip-chip mounted on a flexible substrate ("flex") fabricated by Dyconex, Switzerland.[2] The flex is plugged into a standard socket, as shown in Fig. 7. An opening in the flex substrate is aligned with the sensor and enables free advection. For the flip-chip assembly, 25 μm high gold bumps and a gold frame surrounding the sensor are electroplated onto the chip using the standard bumping process of EM normally used for tape-automated bonding. The electrical interconnections between the chip bumps and the substrate contact pads are soldered with $PbIn_{50}$. In the same fabrication step, the bump frame is soldered to a corresponding structure on the substrate, thus sealing the electronics from the medium flowing over the sensor membrane. Finally an underfill is applied between chip and substrate. The assembly is then inserted into a plastic housing consisting of a cylinder with a 1 mm wide flow channel. The sensor is tangent to the channel. The total volume of the anemometer is 2.8 cm^3. This progress in miniaturization (compared to currently available handheld air flow meters) is due to the unique combination of micromachining, industrial CMOS IC technology, and flip-chip technique.

8. CAD TOOLS

The design of CMOS microtransducers is facilitated by the CAD tools **SOLIDIS**[17] - a simulation toolbox for the numerical modeling of electrical, magnetic, thermal and mechanical effects and their couplings, and **ICMAT** - a data base of process-dependent CMOS materials parameters measured with characterization microstructures of the kind summarized in Section 6. SOLIDIS has been crucial for optimizing the design of the heater/thermopile geometry of the above air flow sensor.[2]

9. ACKNOWLEDGMENT

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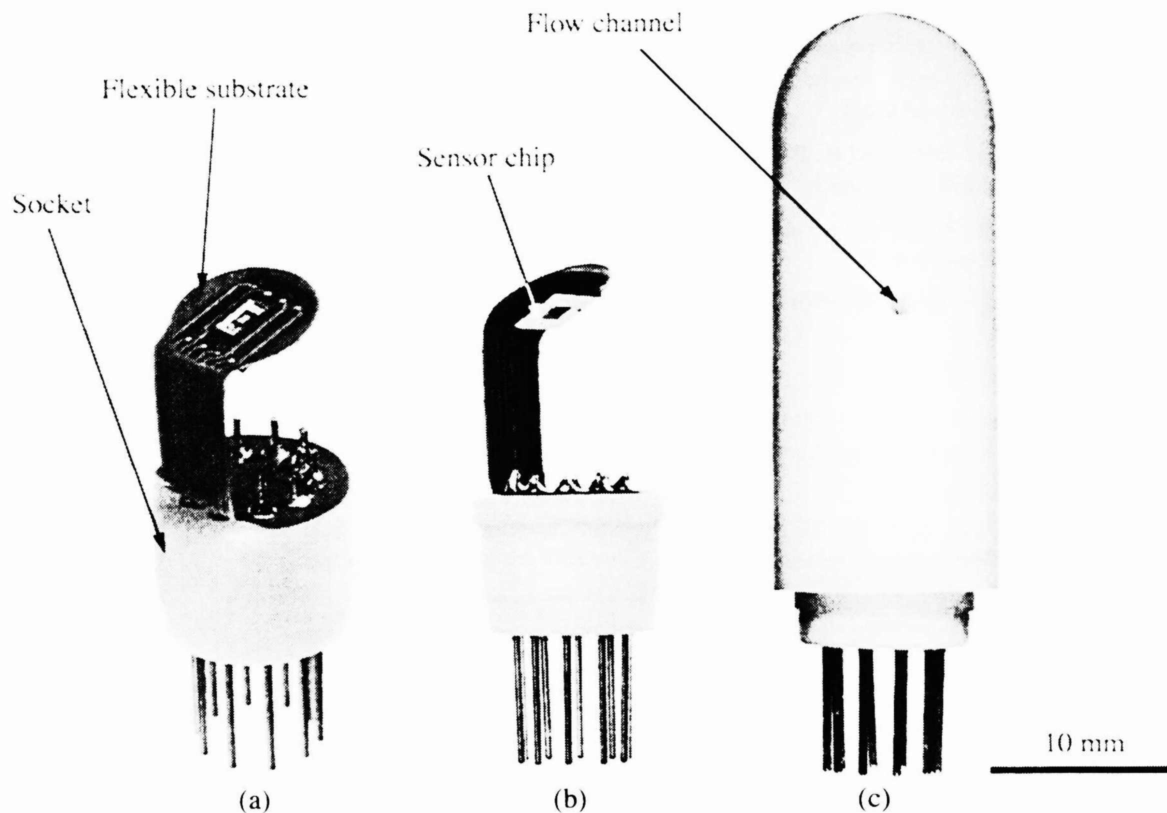

Figure 7: Packaged micromachined flow sensor: chip/flex/socket unit (a, b) before and (c) after insertion into the plastic housing.[2]

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