Metrology for Advanced Transistor and Memristor Devices and Materials

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ABSTRACT

As scaling becomes more challenging, new approaches to transistor design, new materials, and new devices are all being explored. Advanced transistor designs such as vertically stacked nanowire and nanosheet FETs (NW/NS FETs) provide a pathway to sub-10 nm devices. Ferroelectric High K enables extension of FinFET and NW/NS FETs as well as providing a potential dielectric for memristive devices, including RRAM and ferroelectric tunnel junctions. NW/NS FETs provide a significant challenge for both processing and process control due to the geometries associated with their 3D structure. Increasing computational power will ultimately require more than scaling, however. Neuromorphic (brain like) computing and non-Von Neumann computing architectures are now being explored as alternative options for increasing computation capability. To develop efficient neuromorphic and non-Von Neumann hardware, new devices and materials integration strategies are required. This paper provides an overview of advanced NW/NS transistors and new memristor devices and materials and their characterization and metrology.

Keywords: MMSE, scatterometry, Nanowire FETs, Nanosheet FETs, optical metrology

1. INTRODUCTION

As the cost and challenges of further scaling to new technology nodes continue to increase, alternate means of increasing computational capability assume greater urgency. Evidence of this are the “More than Moore” approaches that have been the subject of semiconductor industry road mapping for more than ten years as shown Figure 1 from the International Roadmap for Devices and Structures.(1) New transistor structures that enable increased device packing density, new materials, and new devices are all critical means of achieving this goal. Here we discuss vertically stacked NW and NS FETs, ferroelectric High K, and new memristive memory device with emphasis on their metrology.

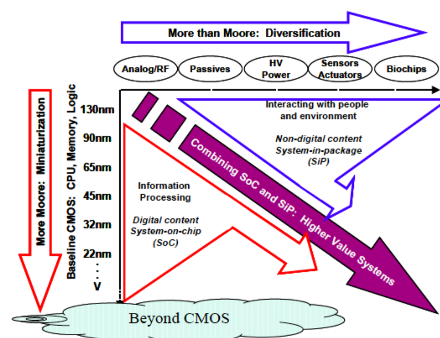

Figure 1. An overview of *More than Moore* approaches to increasing computational capability. Figure from the International Roadmap for Devices and Structures, https://irds.ieee.org/

Vertically stacked nanowire and nanosheet FETs (NW/NS FETs) provide a pathway to sub-10 nm devices by stacking transistor channels instead of spreading them horizontally as is done in planar multi-gate FETs.(2-7) This device design

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increases the challenges associated with measuring decrease feature dimensions.(2-7) NW and NS FET cross-sections are shown in Figure 2. Here, we present two methods that have been used for measuring NW/NS FET structures: Mueller Matrix Spectroscopic Ellipsometry based Scatterometry MMSE-scatterometry and Critical Dimension – Small Angle X-Ray Scattering (CD-SAXS). MMSE-scatterometry is sensitive to cross-polarized light scattering which enables measurement of challenging features including subsurface cavities.(8) Next, Critical Dimension Small Angle X-Ray Scattering (CD-SAXS) is described.(9) The diffraction information obtained by CD-SAXS also provides a means of characterizing subsurface 3D structures critical to these future transistor designs. Examples of characterization capability will include simulations of representative structures as well as experimental measurements of nanowire test structures used to develop etch processes (10).

Increasing computational power will ultimately require more than scaling, however. Neuromorphic (brain like) computing and non-Von Neumann computing architectures are now being explored as alternative options for increasing computation capability.(11) To develop efficient neuromorphic and non-Von Neumann hardware, new devices and materials integration strategies are required. Here we present memristor circuits being fabricated using High K materials, including ferroelectric High K and transition metal oxide resistive random access memory (RRAM). Ferroelectric High K is actively being pursued as a replacement for High K. The negative (differential) capacitance can reduce the voltage required for transistor switching and the dissipated current.(12) This is useful for both 14 nm node transistors and sub 10 nm transistor nodes (12, 13). Ferroelectric High K can also be used in memristor devices (13). Here we discuss the challenges associated with characterizing the crystal phase of these materials. Due to the nanoscale dimensions of the film, synchrotron based X-ray diffraction and extended X-ray absorption fine structure are being used to determine the phases present in these films. We also describe electrical characterization of these films in the context of memristive devices (primarily RRAM, FeRAM and FTJs). These circuits are being designed to mimic the function of synapses in the highly interconnected neuron pathways of the brain. The electrical switching behavior will be shown and with a high-level view of the electrical signals that are used to mimic brain-like behavior (11).

2. Mueller Matrix Spectroscopic Ellipsometry (MMSE) Scatterometry of Nanowire (NW)/Nanosheet (NS) Transistor Structures

Scatterometry is a well-established means of critical dimension measurement. When compared to traditional spectroscopic ellipsometry, MMSE scatterometry increases the ability to measure the 3D profiles of complicated 3D structures. The increased ability of MMSE scatterometry is due to the inclusion of all aspects of light scattering including cross-polarized scattering and depolarization.(8) Furthermore, MMSE provides 16 spectroscopic pieces of information (Mueller matrix elements) vs the two (Psi and Delta) provided by traditional SE which is a key advantage as it provides more structural information about the sample.(8) Here we apply MMSE scatterometry to the characterization of NW/NS test structures used to develop the etch processes used for fabrication of NW/NS FETS. The science and technology of MMSE scatterometry has been previously discussed in the literature and will not be repeated here. (8, 10)

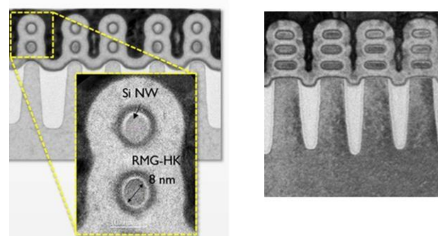

Figure 2. Vertically Stacked Nanowire FET on the left and Nanosheet FET on the left. Figures adapted from references 14 and 15 and copyright IEEE.

Process control for the fabrication of Gate-All-Around (GAA) NW/NS FETs from Si/SiGe/…/Si fins requires measurement of a number of structures that challenge metrology methods. The process flow for NW/NS FETs is shown in Figure 3. Key process steps include the release of the NW/NS channel and the deposition of the High K and metal gate layers. Nanowire test structures are used to develop the selective SiGe etch process used to release the channels, and are shown in Figure 4. Here, we discuss the use of MMSE-scatterometry and CD-SAXS to measure the extent of the selective etch. The results of the MMSE-scatterometry characterization of the selective etch process are shown in Figure 4(d) and for the CD-SAXS characterization in Figures 5 and 6.

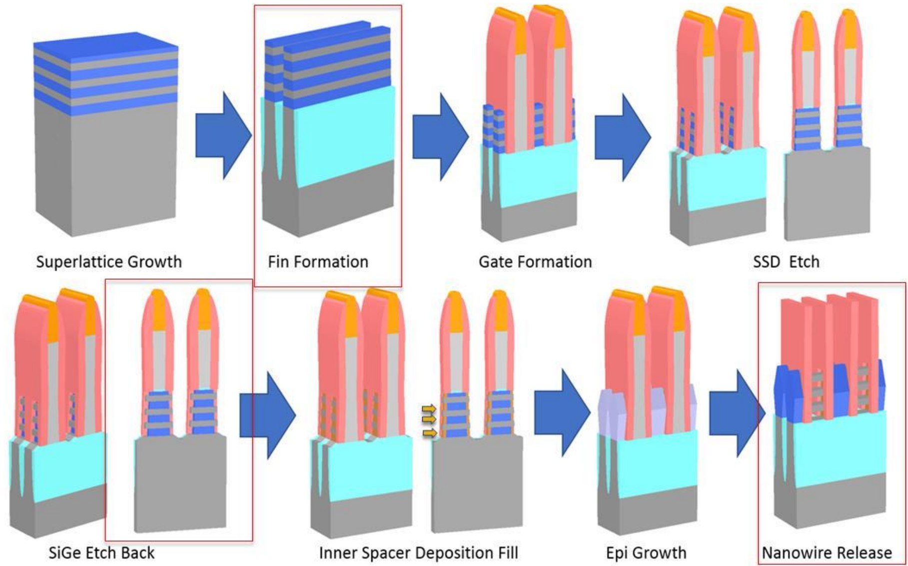

Figure 3. The process flow for fabrication of GAA NW/NS FET. Figure copyright AIP and first published in Ref. 7.

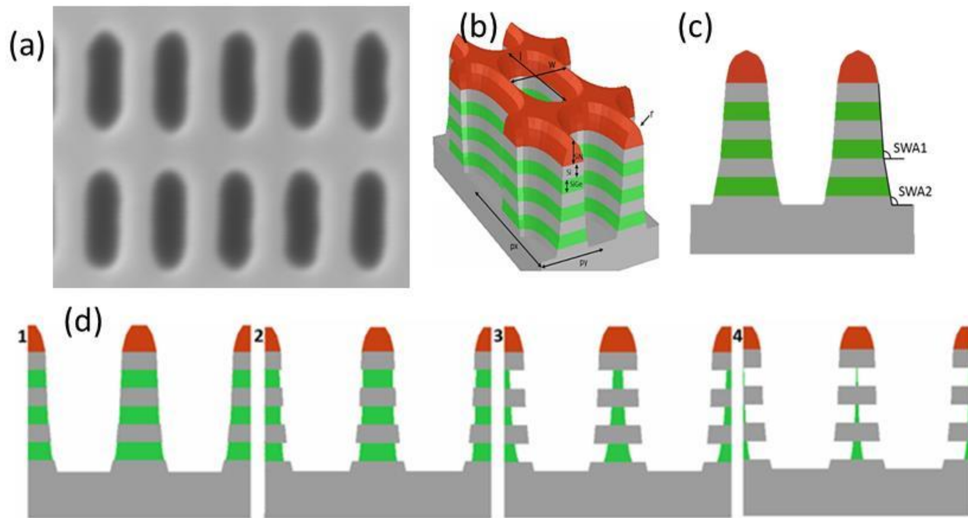

Figure 4. The NWTS and the selective etch of subsurface SiGe layers is shown. A top down view of the holes in the test structure is shown in (a). A section of the optical structure model used for scatterometry simulations is shown in (b). A cross-section along the narrow part of the hole structure is shown in (c). The selective etch of the SiGe subsurface layers is shown in (d). The structures shown in (d) represent a cross-sectional view of the optimized optical model for the selectively etched structures. The amount of selective etch is (1)3.4nm, (2)10.5nm, (3)18.9nm and (4)21.9nm from the sidewall. Figure adapted from Reference 16 with copyright AIP and used with the authors' permission.

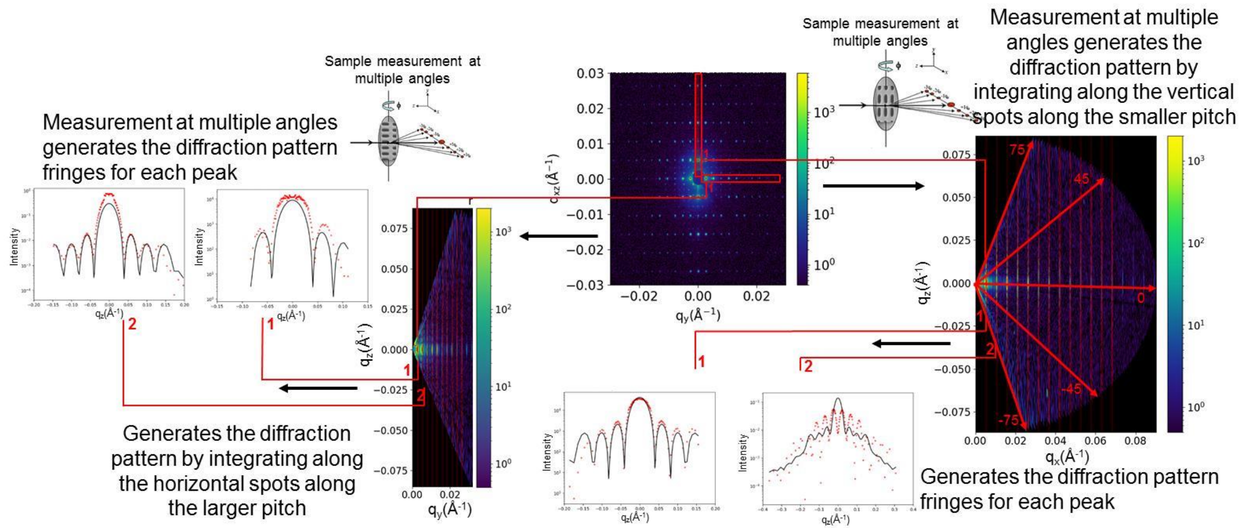

Figure 5. CD-SAXS characterization of the NWTS samples is described. Figure courtesy M. Korde, R.J. Kline, and D. Sunday.

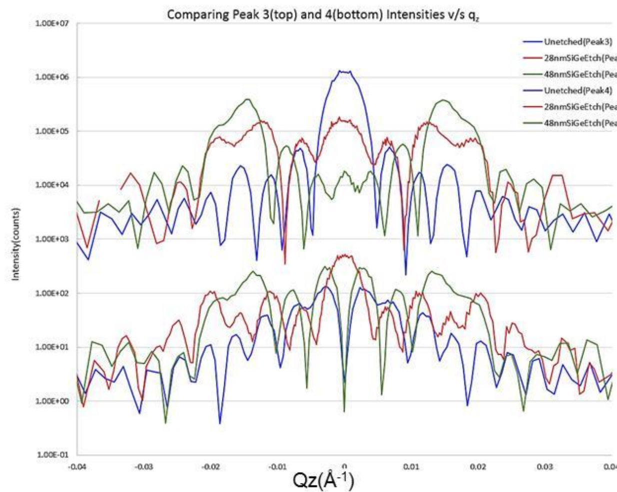

Figure 6. CD-SAXS data showing the sensitivity to selective etching of SiGe layers in the NWTS. The dark blue diffraction data is from the unetched NWTS. The red diffraction data is from the sample having ~ 11 nm etch from the sidewall, and the green diffraction data is from the sample having ~ 22 nm of selective etching from the sidewall.

In addition to reduction in transistor feature dimension and new transistor designs, High K materials continue to advance. The drive to reduce the equivalent oxide thickness resulted in a transition to amorphous hafnium oxide based High K films. This was followed by the use of crystalline higher K hafnium oxide based which included HfZr oxides. The dielectric constant vs crystal phase for Hf oxide is 16 (monoclinic), 29 (cubic), and 70 (tetragonal). Similar trends are observed for HfZr oxide thus driving the need to find processes that resulted in stable higher K phases for the entire gate stack including metal gate. Subsequently, the need to reduce equivalent oxide thickness pushed the use of ferroelectric materials.(12, 13) Ferroelectric dielectric layers such as HfZr oxide provide a negative differential capacitance that reduces transistor operating voltage and power use. (12, 13) Stable fabrication of High K films requires metrology that is capable of determining the crystal phase. Characterization of the crystal phase of the high

K continues to be challenging, especially in-line measurements. Previously, we have shown that synchrotron based grazing incidence in-plane X-Ray diffraction measurement methods can be used to determine the crystal phase as shown in Figure 7.(17) This methodology has been applied to ferroelectric HfZr oxide. In this case, the presence of the ferroelectric phase of HfZr oxide was verified by electrical characterization.(18)

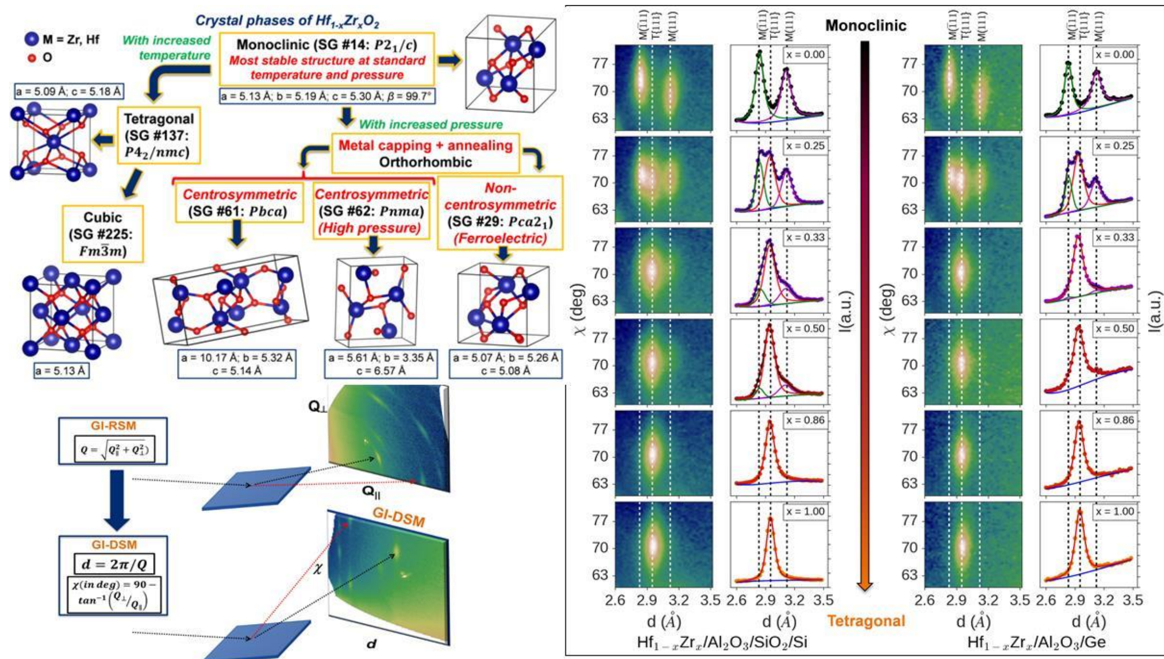

Figure 7. The various crystal phases of HfZr oxide are shown in the upper left. A comparison of GI-I-XRD data in reciprocal space vs d spacing is shown in the lower left. A comparison of the change in crystal phase of $Hf_{1-x}Zr_x$ oxide with Zr concentration x for silicon and germanium substrates is shown on the right. Figure copyright AIP and first published in Reference 17.

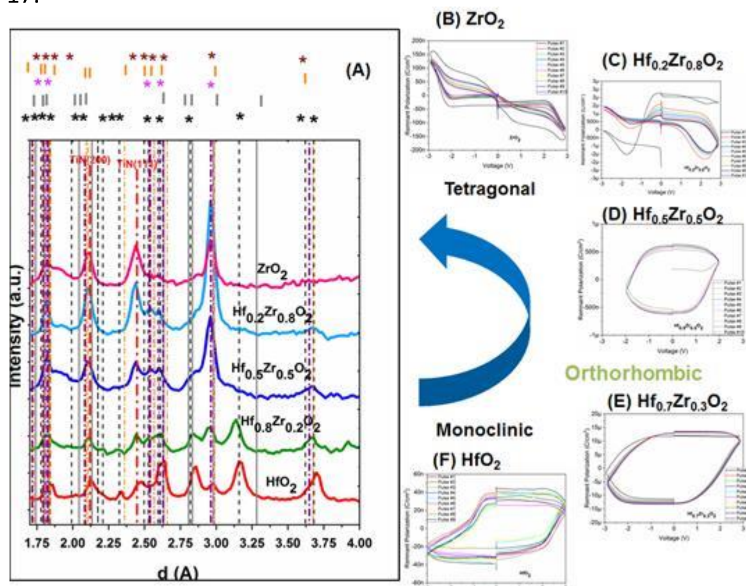

Figure 8. Correlation between crystal phase and electrical characterization of ferroeletric behavior. Figure copyright MRS and first published in Reference 18.

New devices and architectures are also providing challenges to metrology. Since the frequent exchange of information between memory and microprocessor slows overall computation, the need to keep information in the processing unit and have new approaches to memory is driving approaches such as neuromorphic computing based on memristive devices. Memristive devices can be fabricated using traditional silicon processes as shown in Figure 9. Work at SUNY Polytechnic Institute has demonstrated the integration of transition metal oxide based memristors in the first metallization layers of a 65nm CMOS process. (19, 20) To date, both HfO_2 RRAM elements and $Hf_{1-x}Zr_x$ ferroelectric tunnel junction (FTJ) structures have been integrated, specifically at the metal 1 (M1) / via 1 (V1) interface.

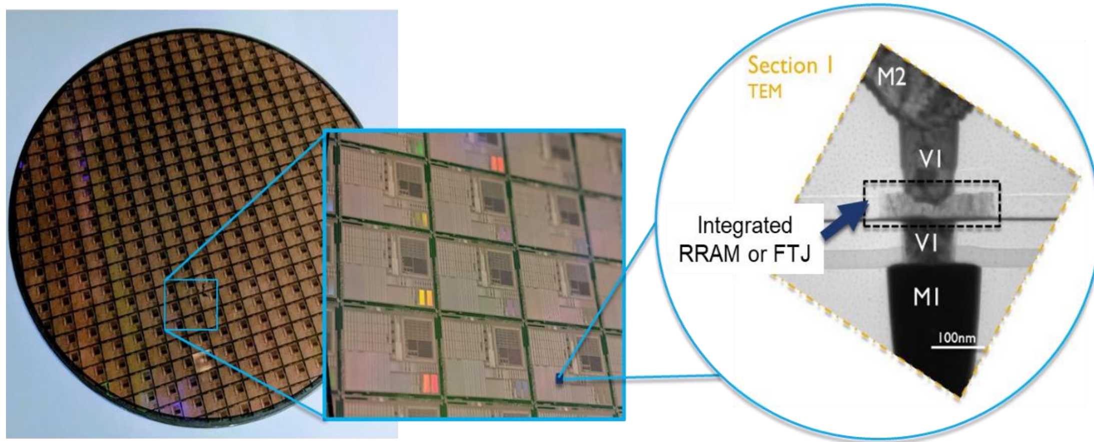

Figure 9. 300mm wafer-scale integration of memristive devices with CMOS. Memristors (including RRAM and/or FTJ) have been integrated at the metal 1 / via 1 interface in a standard 65nm CMOS process.

To demonstrate new architectures, arrays of 1 transistor 1 RRAM (1T1R) elements have been fabricated and tested for multi-bit data storage and so-called "in memory computing". An example of such an array and a visualization of multi-bit memory storage in the array is shown in Figure 10.

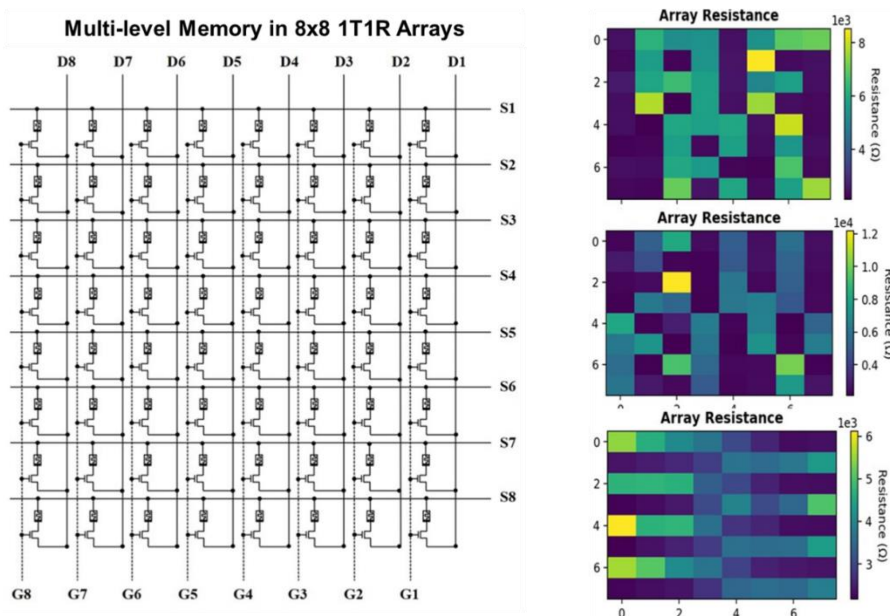

Figure 10. A schematic of an 8x8 1T1R array fabricated at SUNY Polytechnic Institute (left) and a visualization of multi-bit memory storage within that array (right).

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