Integration of EUV lithography in the fabrication of 22-nm node devices

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ABSTRACT

On the road to insertion of extreme ultraviolet (EUV) lithography into production at the 16 nm technology node and below, we are testing its integration into standard semiconductor process flows for 22 nm node devices.

In this paper, we describe the patterning of two levels of a 22 nm node test chip using single-exposure EUV lithography; the other layers of the test chip were patterned using 193 nm immersion lithography. We designed a full-field EUV mask for contact and first interconnect levels using rule-based corrections to compensate for the EUV specific effects of mask shadowing and imaging system flare. The resulting mask and the 0.25-NA EUV scanner utilized for the EUV lithography steps were found to provide more than adequate patterning performance for the 22 nm node devices. The CD uniformity across the exposure field and through a lot of wafers was approximately 6.1% (3σ) and the measured overlay on a representative test chip wafer was 13.0 nm (x) and 12.2 nm (y). A trilayer resist process that provided ample process latitude and sufficient etch selectivity for pattern transfer was utilized to pattern the contact and first interconnect levels. The etch recipes provided good CD control, profiles and end-point discrimination.

The patterned integration wafers have been processed through metal deposition and polish at the contact level and are now being patterned at the first interconnect level.

Keywords: Extreme ultraviolet lithography, EUVL, EUV device integration, EUV OPC, EUV mask, EUV resist process

1. INTRODUCTION

EUV lithography development exhibited significant progress in 2008. The first ever EUV device integration demonstration was carried out using the EUV Alpha Demo Tool in Albany to pattern the first interconnect level on 45-nm test chips[1] manufactured at AMD's fabrication facility in Dresden, Germany. Die-to-die inspection of wafers printed with the EUV device integration mask showed many fewer repeating (mask related) defects than expected given the defect density of the mask blank[2]. The quality of resist images printed with the EUV Alpha Demo Tool in many cases exceeds those that can be printed with 193 nm immersion lithography. The two remaining EUVL technology elements that are at highest risk of not being ready when needed are source power and reliability and mask blank defectivity. Source power and reliability, which is critically important to exposure tool throughput, not only falls far short of what will be required for EUVL exposure tools in a pilot production line but also is only marginally adequate for serious process development work at the present time. However, manufacturers of commercial EUV sources have committed to delivering EUV sources with beta-level performance specifications before the end of the 2009 calendar year[3,4]. Mask

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blank defectivity, which is critically important to the yield of electrically functional devices, greatly exceeds the levels needed for high volume manufacturing (HVM) and given the current rate of progress in blank defect reduction[5] it now seems likely that completely defect-free mask blanks will not be available in the foreseeable future. However, several of the defect workarounds that are now being actively pursued, such as defect compensation and fiducials for blank disposition, may allow functional devices to be manufactured.

The purpose of this paper is to test EUVL readiness via a device fabrication exercise. Such a device demonstration provides the truest test of the technology and at the same time highlights the remaining critical issues. In this paper, we describe the patterning of two levels of a 22 nm node test chip using single-exposure EUV lithography; the other layers were patterned using double-exposure double-etch 193 nm immersion lithography[6]. In Section 2 we present descriptions of the 22 nm node test chip, data correction and mask fabrication, EUV lithography of the contact (CA) and first interconnect (M1) levels, summarize the process steps that take place after EUV lithography, and provide the results of electrical testing at M1. In Section 3, drawing on information available in the published literature and on learning from the current device demonstration exercise, we summarize the current state of EUV lithographic technology. Our conclusions are presented in Section 4.

2. 22 nm EUV DEVICE DEMONSTRATION

The 22 nm node test chips, which utilize high-κ metal gate transistors (L_g = 25 nm) with a contacted gate pitch of 90 nm printed with double-exposure double-etch (DE^2) 193 nm immersion lithography, were described by Haran et al. at IEDM 2008 as containing the smallest fully functional 6T-SRAM cell[7]. In those chips the contact module was patterned using a pitch-split DE^2 process and an aggressive shrink of a trilayer organic resist followed by pattern transfer into the underlying inter-level dielectric to get to a final contact dimension of ~ 26 nm[8]. The metal levels were printed with double-dipole lithography (DDL)[9] and fabricated using a Cu damascene technique. The 22 nm node test chips for the current EUV device demonstration, which utilize devices with a slightly smaller gate pitch (80 nm), were patterned at CA and M1 levels using EUV lithography, as illustrated in Figure 1. All wafer processing for the work described in this paper was carried out at the College of Nanoscale Science & Engineering's (CNSE) Albany Nanotech facilities in Albany, New York.

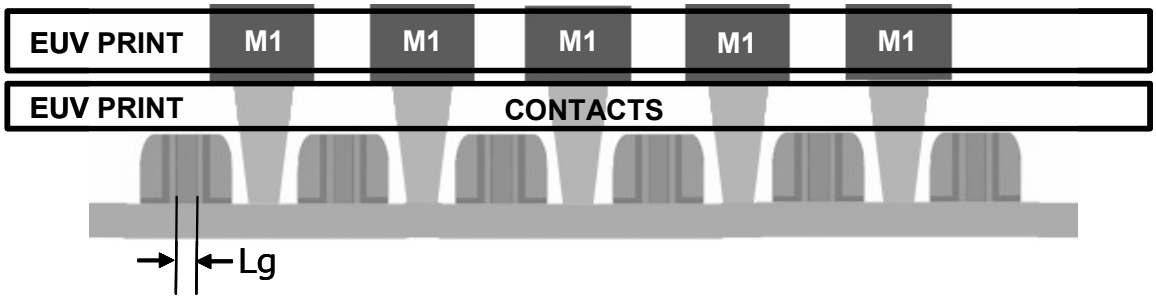


Figure 1– Integrated stack showing all of the levels of the 22 nm node test chip including the contact and first metal layers patterned using EUV lithography.

2.1 Data correction and mask fabrication

The lithographic patterns at the 22 nm node are so small that simple proximity effects such as line end shortening must be corrected using conventional OPC software even when printing with high k_1 (0.74) EUV lithography. Model-based optical proximity correction was applied to the layout data using Mentor Graphics Calibre nmOPC[10] with the following inputs: The EUV exposure tool was assumed to have a 0.25 numerical aperture (NA) imaging system with a centroid wavelength at 13.5 nm and to have a fixed conventional illumination with $\sigma = 0.5$. A simple threshold model was used for the resist and the blur due to acid diffusion was assumed to be 10 nm.

Because EUV imaging systems are reflective, an EUV mask must be illuminated at an angle to its normal, as shown on the left hand side of Figure 2. The interaction of this off-axis light with mask topography causes slight perturbation to

the imaging depending on a features orientation and location in the image field—an effect that is sometimes called the mask shadow effect. The first-order consequence of mask shadowing is a printing difference between horizontal and vertical lines where horizontal is defined as being perpendicular to the plane of incidence formed by the 6 degree off-axis chief-ray and the normal to the mask. Since a horizontal feature consists of perpendicular edges, it will cast a longer shadow than a vertical feature and a horizontal line would therefore appear larger than a vertical line. The required mask adjustment to cause horizontal and vertical lines to print identically (HV Bias) was found experimentally to be 2.8 nm (for line and space pitch values greater than 90 nm)[11], as shown on the right hand side of Figure 3, and via simulation to be 2.2 nm[12]. When correcting the mask data for the 22 nm device demonstration, horizontal lines were made larger by 1.5 nm and vertical lines were made smaller by 1.5 nm and square contact holes were modified so that their vertical dimension was increased by 0.95 nm and their horizontal dimension was decreased by 1.9 nm.

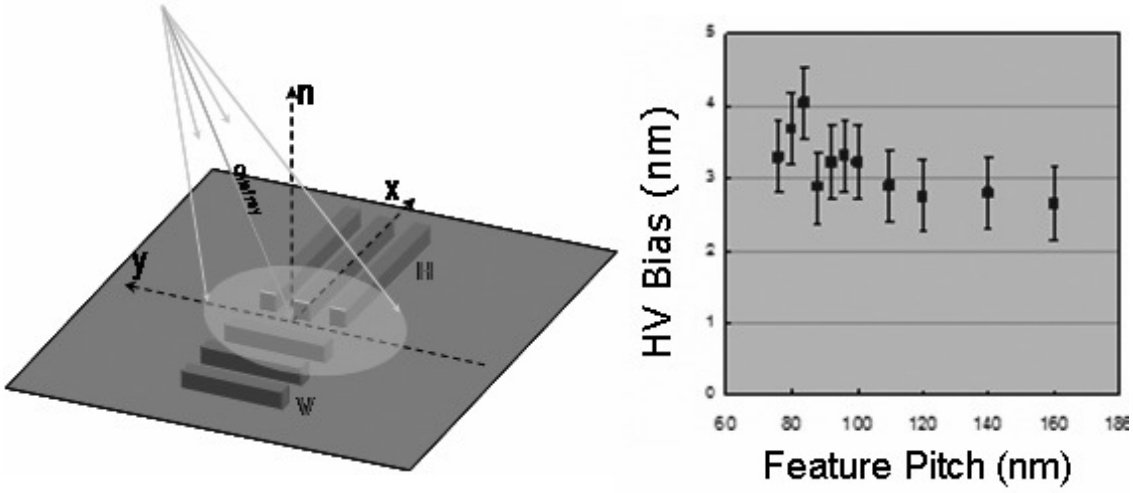


Figure 2 – Illustration of shadow effect caused by non-telecentric illumination of an EUV mask that requires use of HV bias to cause horizontal (H) and vertical (V) lines to print identically. HV bias is approximately 2.8 nm for pitch > 60 nm.

Imaging system flare in the ASML Alpha Demo Tool (ADT) in Albany was experimentally evaluated using a series of donut shaped patterns, consisting of a central post surrounded by a clear annular-shaped field, with different annular radii[13]. The measured point spread function due to flare (spillover parameter versus radius), shown on the left hand side of Figure 3, is seen to fall on a straight line with a slope of minus one, consistent with the slope for the power spectral

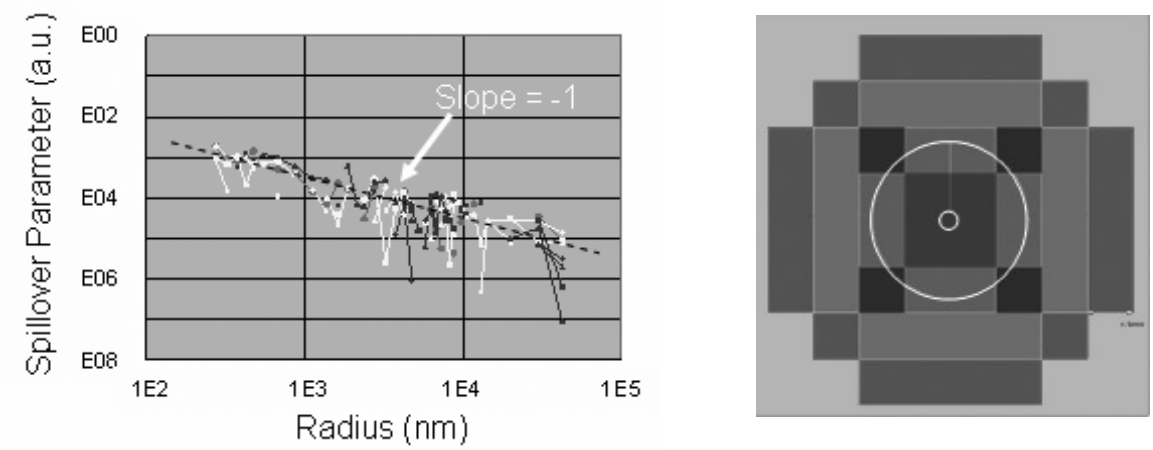


Figure 3 – EUV flare effect: Measured point-spread function due to flare and density map of mask area containing an annular-shaped feature that is used to adjust the position of feature edge.

density (PSD) due to mirror surface roughness[14]. The experimental flare data shown on the left hand side of Figure 3 were fit to a double Gaussian function which was used to create a density map of the mask layout using the Mentor Graphics Calibre DENSITY CONVOLVE function. The density map of a donut shaped pattern consisting of a 200 nm

diameter isolated post surrounded by a 0.75 μm clear annulus (like the pattern that was used to collect the experimental flare data) is shown on the right hand side of Figure 3, as an example. The measured flare data from the donut pattern was compared to simulation results to create a lookup table which was subsequently used to adjust the edge position of every feature in the layout according to the density layer in which it fell.

The mask data for the 22 nm contact level was corrected for conventional OPC and for mask shadowing using the methods described above. The impact of flare correction on the printed size of contacts was minimal, because the density of contact holes was quite small. The mask data for the first interconnect level was corrected for conventional OPC, mask shadowing, and imaging system flare. The corrected mask data was provided to the Advanced Mask Technology Center (AMTC) in Dresden, Germany for use in fabricating the mask. The mask was built using a ULE 6025 blank from Schott Lithotec AG with a 11 nm thick Si-capped MoSi multilayer, a 10 nm thick SiO_2 buffer layer, and a 67 nm thick TaN absorber.

2.2 EUV printing of the CA and M1 levels

The EUV lithography steps were carried out using the ASML Alpha Demo Tool (ADT)[15] located at Albany Nanotech. This full-field EUV scanner has a centroid wavelength of 13.5 nm, a numerical aperture (NA) of 0.25, and a conventional illumination system with a pupil fill of $\sigma = 0.5$. The resist system used for all of the lithographic steps reported in this paper was SEVR 40, which is produced by Shin-Etsu MicroSi, Inc., and had been previously shown by the authors using the EUV Micro-Exposure Tool (MET) in Berkeley to have adequate patterning performance for the 22 nm logic node[16].

The process latitude when printing dense arrays of 45 nm contact holes in a 100 nm thick film of SEVR 40 resist using the ADT is shown in Figure 4. At ~5% exposure latitude the depth of focus (DOF) was 245 nm. The corresponding Bossung plot is also shown in Figure 4. The dose-to-size for 45 nm diameter contact holes was 47.6 mJ/cm^2.

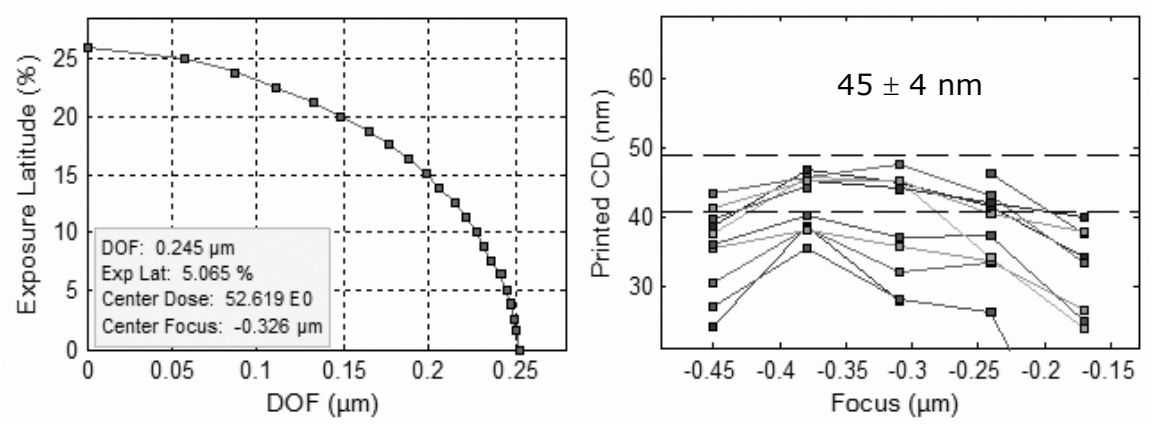
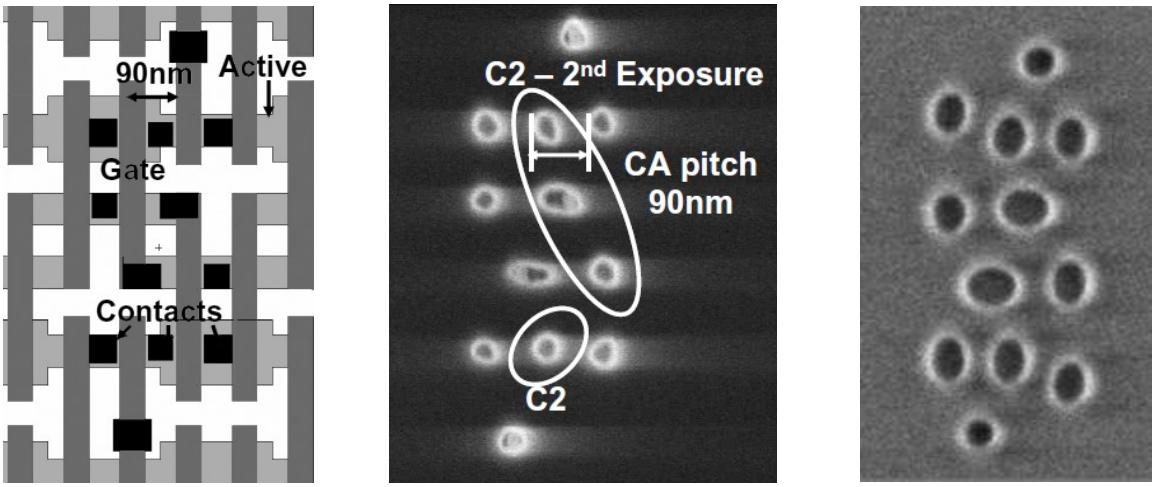


Figure 4 – Performance of 100 nm thick film of ShinEtsu SEVR-40 resist. (a) Exposure latitude for 45 nm diameter contact holes. (b) Corresponding Bossung plot.

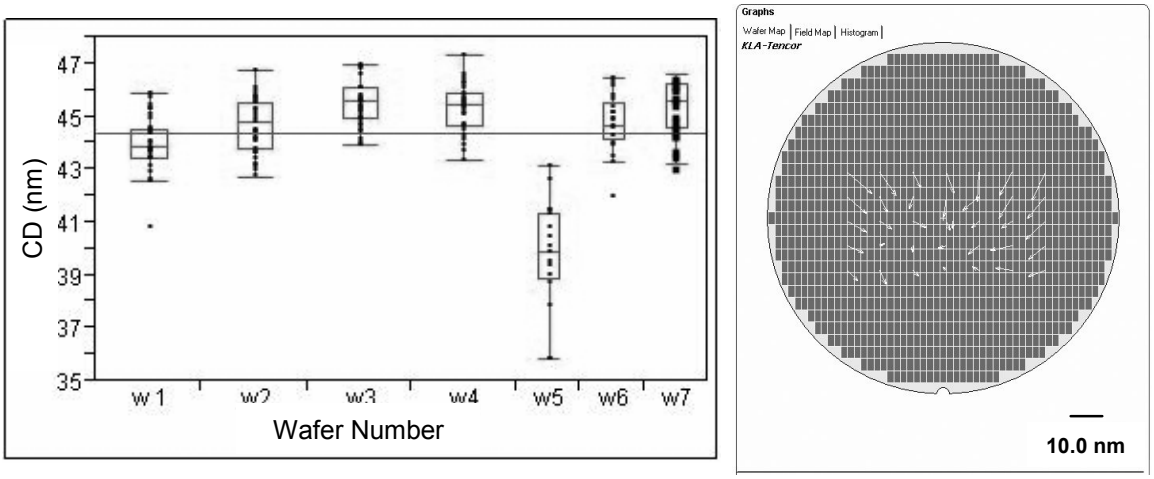
The quality of the contact hole resist images in 100 nm thick films of SEVR 40 resist at the dose-to-size and at best focus is illustrated in Figure 5. In addition to top-down images of the CA level of the 80 nm pitch 0.08 μm^2 6T-SRAM flycell and an area of the 0.08 μm^2 6T-SRAM bit cell array, Figure 5 also shows the arrangement of the active area, gate, and contacts for the 22 nm node SRAM fly cell.



(a) (b) (c)

Figure 5 – (a) Layout of 22 nm node 0.1 μm^2 SRAM flycell. (b) Resist image of contact level of 80-nm pitch SRAM flycell printed using EUV lithography. (c) Resist image of contact level of 80 nm pitch SRAM bit cell printed using EUV lithography.

A more quantitative assessment of the imaging of the 22 nm node test chips using the ADT is provided by the control of the features critical dimension (CD) across the wafer for the entire lot of wafers. A CD control chart showing all CD measurements for 7 exposed wafers is shown in Figure 6 (a). The mean CD is 44.9 and the variation (when data for w5

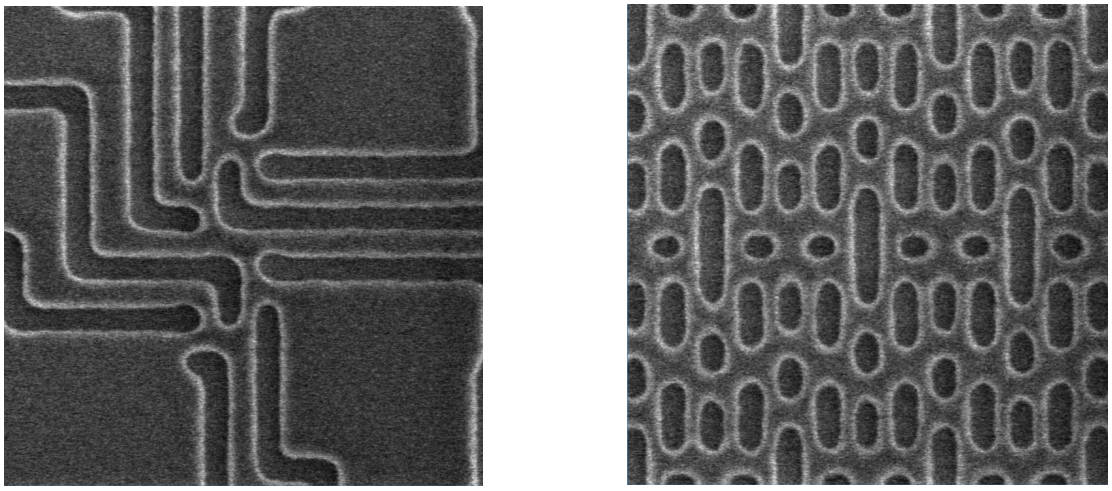


(a) (b)

Figure 6 – (a) CD control chart of 7 wafers printed on the EUV scanner. The mean CD is 44.9 nm and the variation (when the data for w5 is excluded) is 6.1 % (3σ). (b) Wafer map of overlay results between the contact layer patterned with EUV lithograph and the previous layer patterned with 193 nm immersion lithography. The mean + 3σ overlay values are 13.0 nm in the horizontal direction and 12.2 nm in the vertical direction.

is excluded) is 6.1% (3σ). The other important metric for the EUV lithography step in this integration exercise is the value of on-product overlay. A wafer map of some representative overlay results between the CA layer printed with EUV lithography and the previous layer (PC) patterned with 193 nm immersion lithography is shown in Figure 6 (b). The mean + 3σ overlay values were 13.0 nm (x) and 12.2 nm (y). If field-by-field corrections were to be applied, the modeled residual overlay errors could be as low as 4.2 nm (x) and 4.9 (y). As expected, the matched-machine-overlay numbers are significantly higher than the typical single machine overlay numbers for the ADT, typically ~ 4 - 5 nm in both x and y.

Some representative EUV resist images of the first interconnect level (M1) of the 22 nm node test chip in 100 nm thick films of SEVR 40 resist are shown in Figure 7. A top-down SEM image of the M1 level pattern of the 0.08 μm^2 6T-SRAM test structure (flycell) is shown in Figure 7 (a) and an area of the SRAM bit cell are shown in Figure 7 (b).



(a) (b)

Figure 7 – (a) Resist image of first interconnect level of 0.08 μm^2 6T-SRAM flycell. (b) Resist image of first interconnect level of 0.08 μm^2 6T-SRAM bit cell.

EUV resist images of the M1 level SRAM flycell with and without mask shadow corrections are shown in Figure 8. As described in Section 2.1, to correct for mask shadowing a simple HV bias of about 0.75 um was applied to each edge.

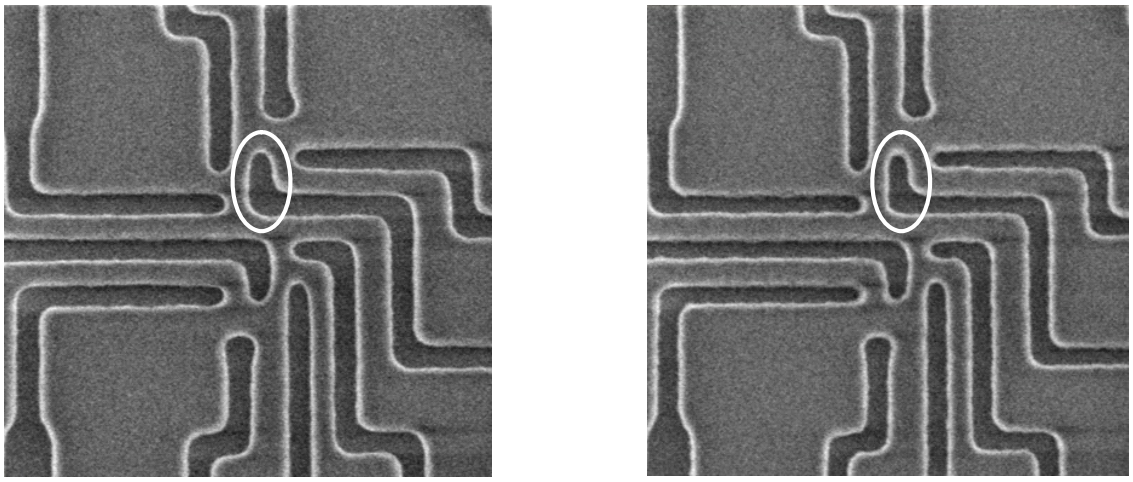
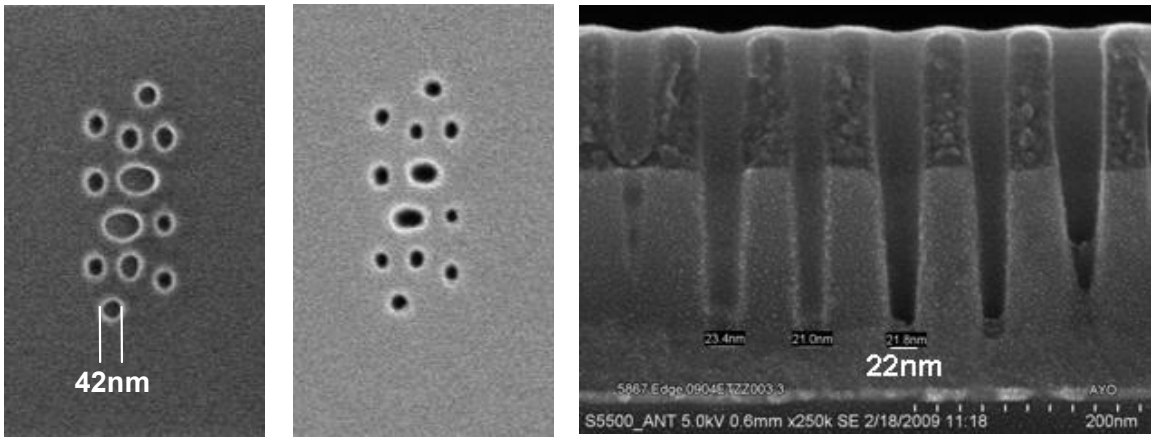


Figure 8 – Resist images of first interconnect level of 80 nm pitch SRAM flycell with and without correcting for mask shadow effect. A constant HV bias rectifies horizontal and vertical lines but is not able to improve the quality of small 2 dimensional features (circled).

In the image on the left, the presence of such an HV bias appears to have resulted in a noticeable improvement in the balance between horizontal and vertical features. However, in the image of the two-dimensional "claws" near the center of the image on the right, the application of a constant HV bias was obviously not helpful. This result suggests that more accurate resist models, higher scanner reproducibility, and model-based rather than rule-based corrections for mask shadowing will be needed at future lithography nodes.

2.3 Additional processing steps

The next steps in the device integration demonstration involved the transfer of the EUV resist images of the CA level into the underlying layers. The resist patterns were first transferred into a silicon-containing BARC and then into an organic planarizing-layer using reactive-ion-etching before the inter-level dielectic was etched to produce a final contact diameter of ~ 26 nm and a novel Cu metalization scheme was used to fill the high-aspect-ratio contacts. Top-down SEM images of the 12 contacts in the 0.08 μm^2 6T-SRAM single-cell test structure post litho and post oxide-etch are shown in Figure 9. A cross-sectional SEM of the contact holes post-oxide-etch is also shown in Figure 9. The lot of integrated

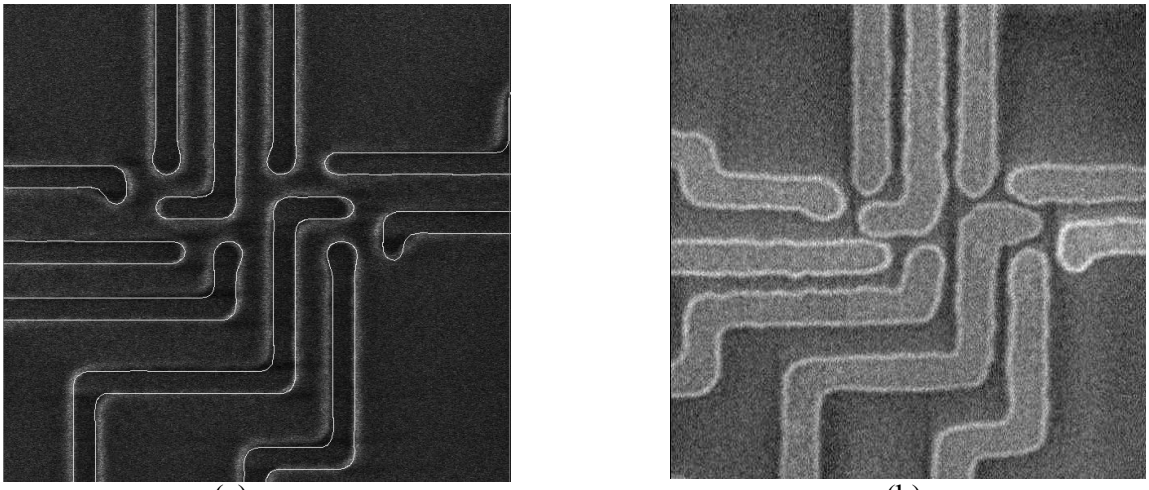


(a) (b) (c)

Figure 9 – Etch process: (a) Resist image of contact level pattern for 0.08 μm^2 SRAM flycell printed with EUV lithography. (b) SEM image of the same pattern in oxide after etch transfer. (c) Cross-sectional SEM image of the contact holes with bottom diameters close to the 25 nm target.

device wafers has been processed through contact metallization and polish and is ready for the M1 damascene patterning and Cu Fill/CMP steps which must be completed before electrical testing of the devices will be possible. At this point in the processing, the contact metalization appears to have been successful and the via-chains seem to be defect free.

In parallel with the contact patterning and metallization work, considerable progress has been made on the EUV patterning of the M1 level. Top-down SEM images of the M1 level of the 0.08 μm^2 6T-SRAM single cell test structure post EUV lithography and post etch are shown in Figure 10. A 6 wafer lot of M1 stack wafers has been patterned



(a) (b)

Figure 10 – (a) Resist image of first interconnect level of 0.08 μm2 SRAM flycell printed with EUV lithography overlaid with a contour from the OPC simulation. (b) SEM image of the same pattern following etch transfer, Cu deposition and CMP.

using EUV lithography and ~40 nm wide metal lines have been fabricated using a Cu damascene technique. These wafers are currently waiting for the results of electrical testing.

2.4 Electical testing at M1

The best indication of the successful integration of EUV lithography in the fabrication of 22-nm node devices comes from the electrical tests of the devices under construction. Some examples of the structures that are present at M1 designed to test resistance, and parasitic capacitance and detect opens and shorts are shown in Figure 12.

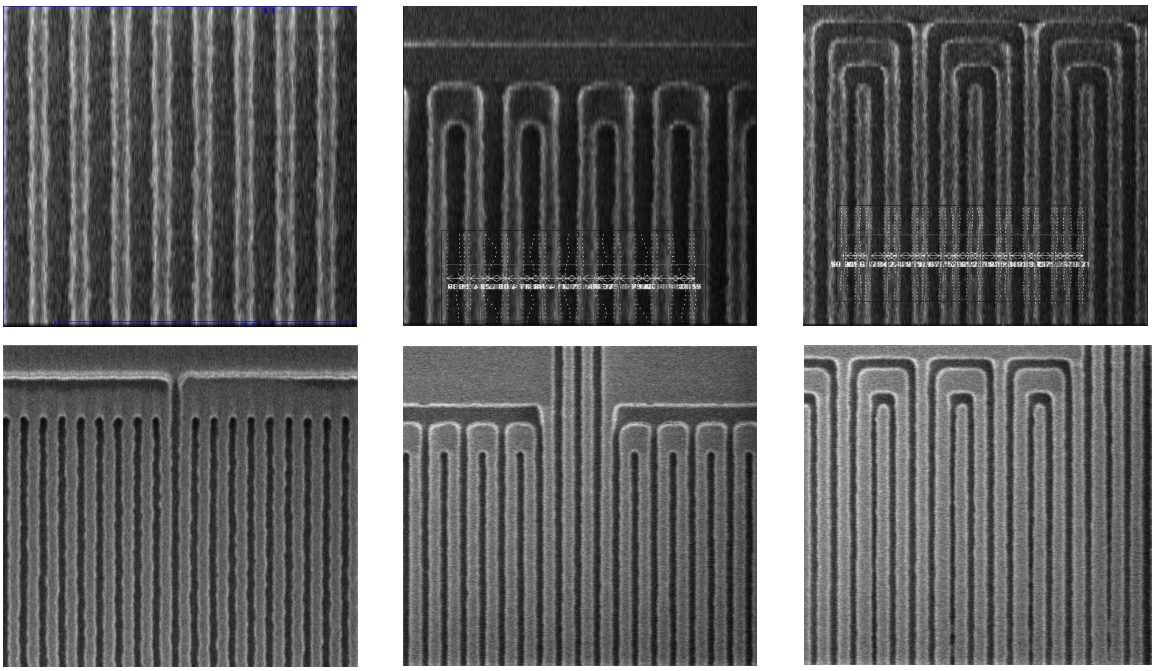
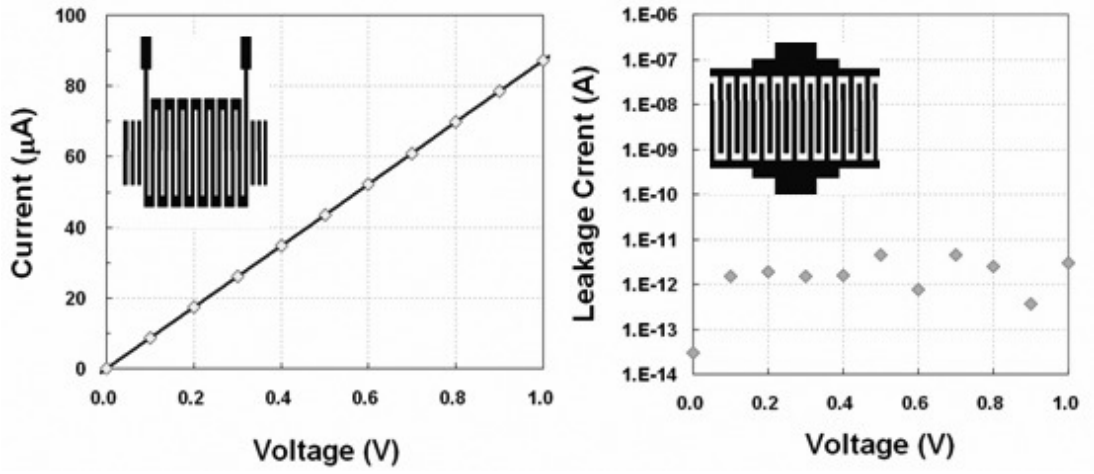


Figure 11 – SEM images of first interconnect level patterns after EUV lithography (top) and after etch transfer (bottom) that will be used to measure resistance, capacitance, opens and shorts following copper deposition and polish.

Two examples of the experimental data that was obtained from the M1 level patterns shown in Figure 11 printed with EUV lithography following copper deposition and polish are shown in Figure 12.



(a) (b)

Figure 12 – Plot of current versus voltage from (a) two point resistor macro showing good resistance linearity for 40 nm copper lines and (b) comb macro showing that there is no leakage current between the two 40 nm combs

3. EUVL TECHNOLOGY ASSESSMENT

This section summarizes the current status of EUV lithography technology and compares current values of the most important metrics for each of the critical elements of the technology to the values that will be needed for EUVL pilot production at the 15 nm node.

The current status of the two leading EUV source technologies, discharge-produced plasma (DPP) and laser-produced plasma (LPP) is as follows: 8 Watts of in-band power at intermediate focus (IF) has been demonstrated over many hours of operation by combining a 170 W/2pi DPP source with a full debris-mitigation-system and a 6-shell grazing-incidence collector[4]; 45 Watts of in-band power at IF in 400 msec long bursts has been produced by combining a CO_2 LPP Sn droplet source with a 5 sr normal incidence collector[3]. The current source requirements, 115 W at IF, an etendue limit of 3 mm^2sr and a repetition rate of 10 kHz or higher[17], are very severe and significant progress still needs to be made to achieve the performance required for HVM while still maintaining an acceptable cost of ownership for EUVL. For the later stages of HVM EUV sources with up to 400 W of power at IF are likely to be needed.

The current champion blank defect density, ~ 0.04 defects/cm^2 at 53 nm inspection sensitivity, which corresponds roughly to 0.4 defects/cm^2 when scaled to 25 nm defect size, is approximately 100 times larger than that needed for HVM but is approaching the level needed for a EUVL pilot line. At the present time, the blank defect density numbers on the best blanks is dominated by defects that originate from substrate pits and bumps. The rate of progress in blank defect reduction is currently limited by the performance of available inspection tools. Given the current rate of progress in blank defect reduction, it now seems likely that completely defect-free blanks will not be available any time soon. Because of this, the most promising blank defect "workarounds" which include defect avoidance and defect compensation, both of which require accurate data on defect locations, are almost certainly going to be needed.

The current status of EUV resist materials is quite encouraging with 6 of the leading commercial resist supplier now able to supply resist materials that provide dense line and space resolution better than 28 nm, sensitivities in the 7.5 – 15 mJ/cm^2 dose range, and LER values below 3.5 nm (3σ)[18]. However, it now seems likely that the use of smoothing underlayers, special rinse liquids, and/or smoothing during etch transfer will be required to ensure the LER performance needed for pilot production at the 15 nm node.

The quality of EUV projection optics, particularly those fabricated by Nikon[19], already exceeds that needed for a 15 nm pilot line exposure tool. All three suppliers of EUVL exposure tools are assembling at-wavelength EUV wavefront metrology system to align and qualify the projection optics in their next generation of EUV exposure tools. According to ASML's EUVL tool roadmap[20], two of their EUVL tools will be in production in 2011, the NXE: 3100 (pre production) tool, which has a 0.25 NA imaging system, will support 4 nm OVL, and provide a throughput of ~ 60 wafers per hour, and a first generation volume production tool, which has a 0.32 NA imaging system, will support 3 nm OVL, and provide a throughput of ~ 150 wafers per hour. According to Nikon's EUVL tool roadmap[21], their first HVM tool, the EUV3 with NA > 0.3 projection optics, will be available in 2012 and according to Cannon's EUV tool roadmap[22], their first HVM tool, the VS2 with NA > 0.32 projection optics, will be available in 2015. Once EUVL is inserted into production, all three exposure tool suppliers expect the technology to make use of higher NAs and lower k_1 values to access all of the remaining nodes on the ITRS roadmap.

4. CONCLUSIONS

EUV lithography with the 0.25 NA Alpha Demo Tool has successfully been used to print CA and M1 levels on 22 nm node test chips. The quality of EUVL printing at the 22 nm node is considerably higher than the printing produced with double-exposure double-etch 193-nm immersion lithography as expected for this higher k_1 imaging solution (particularly for 2D imaging). Source power and reliability and mask defectivity are the most serious remaining EUVL critical issues and the power that can be provided by current sources has only recently reached the level needed for serious process development. Mask defectivity is not as bad as was expected given blank defect levels, but is considerably higher than the level needed for HVM. Recent progress in EUV resist development has been outstanding and the performance of state-of-the-art resists is now sufficient for 22 nm node pilot production.

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