REVIEW

Review of nanosheet metrology opportunities for technology readiness

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Abstract. Over the past several years, stacked nanosheet gate-all-around (GAA) transistors captured the focus of the semiconductor industry and have been identified as the lead architecture to continue logic complementary metal-oxide-semiconductor scaling beyond 5 nm node. The fabrication of GAA devices requires specific integration modules. From very early processing points, these structures require complex metrology to fully characterize the three-dimensional parameter set. As the technology progresses through research and development cycles and is poised to transition to manufacturing, there are many opportunities and challenges that still remain for in-line metrology. Especially valuable are measurement techniques that are non-destructive, fast, and provide multi-dimensional feedback, where reducing dependencies on offline techniques has a direct impact on the frequency of cycles of learning. More than previous technologies, then, nanosheet technology may be when some offline techniques transition from the lab to the fab, as certain critical measurements need to be monitored in real time. Thanks to the computing revolution the semiconductor industry enabled, machine learning has begun to permeate in-line disposition, and hybrid metrology systems continue to advance. Of course, metrology solutions and methodologies developed for prior technologies will also still have a large role in the characterization of these structures, as effects such as line edge roughness, pitch walk, and defectivity continue to be managed. We review related prior studies and advocate for future metrology development that ensures nanosheet technology has the in-line data necessary for success. [DOI: 10.1117/1.JMM.21.2.021206]

Keywords: nanosheet; gate-all-around; metrology; characterization.

Paper 21090SSV received Oct. 31, 2021; accepted for publication Mar. 15, 2022; published online Apr. 18, 2022.

1 Introduction

The semiconductor industry has been built upon scaling innovations for generations of complementary metal-oxide semiconductor (CMOS) logic technology nodes, following the widely known Moore's law. Each successively smaller node has been challenging the limits of what research and manufacturing can jointly accomplish and faced increasing skepticism about its success. The scaling paradigm aims to fit as many transistor elements in a region as possible, shrinking the lateral dimensions to achieve increasingly smaller features. Recent logic technologies' success has been reached through many clever processing innovations, design technology co-optimization, and the maturity of extreme ultraviolet (EUV) lithography for production-scale throughput and stability.[1] While the technical accomplishments are demonstratively better than prior nodes, so too were the financial investments higher, time to manufacture longer, and engineering development larger than ever before.[2]

Device architecture and scaling play complementary roles in the industry's history, with architectures setting the framework and scaling taking over until it runs out of steam. After key engineering accomplishments like stress engineering and high-k (HK) metal gates, metal-oxide-semiconductor field effect transistors (MOSFETs) reached their limits and the new fin field-effect transistors (finFETs) took over.[3] FinFETs have had their own evolutions toward greater performance through multi-patterning and aspect ratio advancements, but over recent years,

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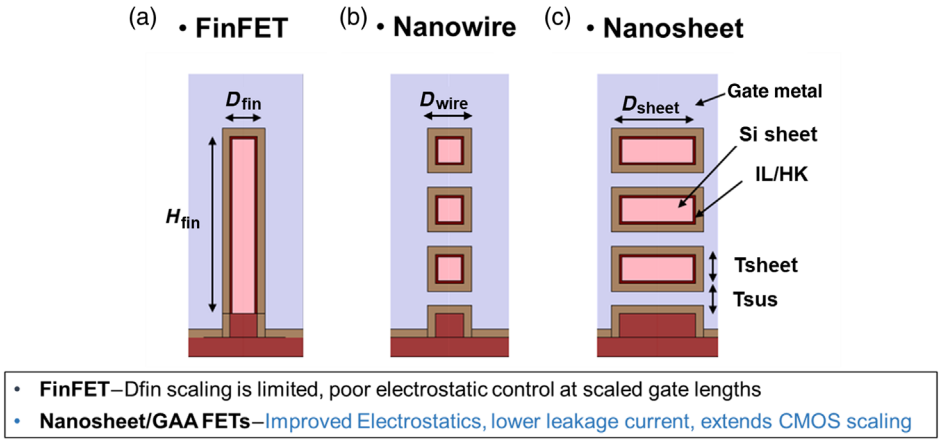

Fig. 1 Comparison of dimensional elements for (a) FinFET, (b) nanowire, and (c) nanosheet devices.[9]

nanosheets have gained momentum as the next leading architecture.[4] IBM made the first major demonstration of nanosheet readiness in 2017,[5] and following years of development, IBM has proven a high-performance computing (HPC) technology to lead the 2-nm node.[6]

1.1 *What Are Nanosheets?*

Nanosheets fall in the family of gate-all-around (GAA) devices, which had been studied in the industry for decades.[7] A predecessor of nanosheets—nanowires—are also a topic of study,[8] but nanosheets have proven superior in many critical aspects and gained most of the attention in this device category. As shown in Fig. 1, all three architectures feature a Si interior (pink) surrounded by a conformal combination of an interlayer dielectric film and an HK film. FinFETs have three free surface planes which are surrounded by the gate when it is patterned perpendicular to the fins. Nanowires, shown in the center graphic, generally have a small volume relative to the surface area and are surrounded by the gate on all four sides of each wire. Nanosheets extend these two concepts into rectangular sheets that are stacked vertically, increasing the available surface area and the channel width.

The optimal number of sheets for a GAA device has been broadly accepted in the industry at three sheets, and one of the most cited papers on the topic was by Lauer and colleagues in 2015.[10] Their study shows that increasing from one-stack to two-stack has a significant gain (>35%) in performance, while an increase from a two-stack to three-stack arrangement does improve, but by much less (~10%). Not only does increasing the number of sheet stacks show diminishing returns, but it also increases the process complexity, which would require further engineering development.

Another component of Lauer's 2015 data speaks to the impact of the wire dimensional scaling (D_{wire}) on performance, with a key message being that no matter the sheet stack, improved electrostatics come at larger fin widths.[10] This is also validated by Kim et al.,[9] whose results compare the frequency achieved by finFETs and nanowires of varying heights (H_{fin}/T_{wire}) as they scale dimensionally (D_{fin}/D_{sheet}). Like Lauer's results, at the smallest fin dimensions, finFETs perform better, while nanowires improve at wider widths (D_{sheet}). Owing to these width-driven improvements, nanosheets had overtaken the nanowire which is fundamentally narrower. An advantage of nanosheets is that the three-dimensional nature provides a wider parameter space (lateral sheet dimensions and thickness) to tailor the transistors for a broad range of performances. Kim et al.'s work shows that at increasing fin widths, the spread in the sheet height performance increases, and the best performance is achieved with thinner sheets at wider dimensions.

2 Nanosheet Process Flow

The general overview of the process flow is described by Loubet et al.[5] in Fig. 2. The patterning phases follow a more traditional front-end-of-line (FEOL) sequence but interspersed throughout

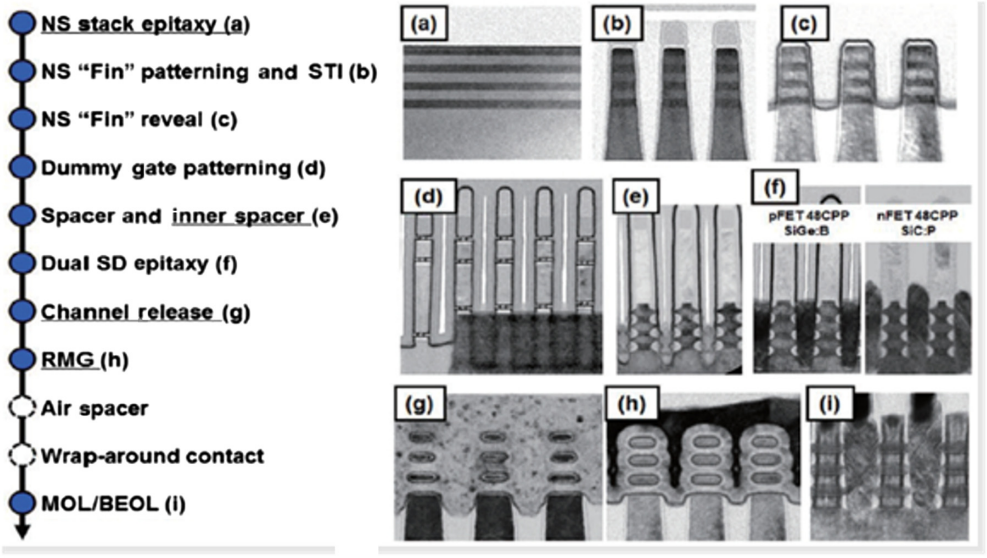

Fig. 2 Critical nanosheet process steps from a common integration scheme with corresponding cross-section images showing the structural evolution.[5]

are new processing steps to form and engineer the sheets. Nanosheet device fabrication begins by epitaxially growing alternating silicon and silicon-germanium (SiGe) layers, which are generally on the order of 5- to 20-nm thick,[5] on a blanket silicon wafer. The SiGe layers are sacrificial in the presented process and will eventually be removed, but they are a critical element for the main process sequences in this common integration scheme. This step defines the T_{sheet} for the devices, and as discussed earlier, thinner is better for electrostatic performance. Thickness control is shown to be excellent via epitaxial growth.[11] Due to the lattice mismatch between Si and SiGe, the SiGe layers are strained, but the strain of each sheet can evolve through the patterning and processing flow.[12] In the final device, the carrier mobility will be affected by this eventual strain in the p-channel FET (PFET) and n-channel FET (NFET) devices.

Following stack growth, the sheet width (D_{sheet}) is defined in a process similar to fin patterning, creating "fins" [Figs. 2(b) and 2(c)]. Further stages may trim the sheets, but as discussed in Kim et al.,[9] wider sheets provide the best performance. Vertical sidewall angles are preferred to more tapered profiles, to minimize variability in sheet widths within a single fin and maximize width at the top sheet where a taper would traditionally have the most width lost. Roughness on any surface can also impact the sheet dimensions, so patterning processes that generate smoother sidewalls and low line edge roughness (LER) and line width roughness (LWR) help minimize variability.

The next series of steps [Fig. 2(d)] generate the dummy gate, which is a critical stage where the second lateral sheet dimension is defined (channel length L_g). The same roughness and sidewall angle concerns exist for the gate as for the fins, as any variation would have performance impacts. A recent technology computer-aided design simulation study by Sriram and Bindu[13] for MOSFETs with 500 LER permutations for devices with a 30 nm gate estimates a standard variation in threshold voltage (V_T) of 6.4 mV. While not directly applicable to nanosheets, one can expect similar or worse variation given the increased complexity of the nanosheet technology. As shown in the image corresponding to this phase, the dummy gate tends to be a high-aspect-ratio feature due to the integration required for the process flow.

The next module in the nanosheet flow [Fig. 2(e)], "spacer and inner spacer," involves depositing a spacer, cutting the unwanted, exposing sections of fins, and laterally etching back the sacrificial SiGe sheets to form an indent. The indent is accomplished through highly selective etch,[14] which ideally leaves the Si sheets unaltered to retain their sheet width. Etch rate is shown to vary with Ge content,[15] which is yet another reason why monitoring the Ge content through the process flow is important. Too shallow an indent may not effectively isolate the source/drain region from the channel, while too deep of an indent may leave no space for the channel and severely shorten the effective gate length, L_g.

This indent is then filled by the inner spacer, leaving only the Si sheets exposed on the sidewall for the source/drain epitaxial growth in the following process stage. The inner spacer also serves a purpose in even later modules by protecting and isolating the channel, so shallow inner spacer growth could reduce the effectiveness as insulation. The spacer is then trimmed, and incomplete trimming can leave some spacer covering the Si sheets, which would shield the Si and prevent subsequent epitaxial nucleation.

Following the inner spacer process, the source/drain (S/D) epi is preferentially grown where the Si sheets are exposed in between gates [Fig. 2(f)]. There are three main criteria the epi process must accomplish:[16]

1. Epi nucleation and growth are needed on all three sheets to ensure connectivity.
2. Epi height cannot be too tall or may impact future processing steps.
3. Epi must merge fully along the trench to ensure connectivity.

Care must be taken as epi growth can be a sensitive process to develop and control. Criteria 1 and 2 of the above list are represented graphically in Fig. 3(a), where the ideal epi fills the trench, connects all three sheets and stops above the top sheet. Non-ideal epi growth either overfills the trench, which can cause downstream processing issues, or underfills. Situations with underfill arise from epi not successfully nucleating on all three sheets, which can cause visible undergrowth or hidden voids, and undergrowth of the epi that does not bridge the space between dummy gates. Epi merge quality can be understood from the along-trench epi growth level, depicted top down in Fig. 3(b), and from a cross-section perspective in Fig. 3(c).

The next major process sequence, channel release [Fig. 2(g)] involves fully removing both the dummy gate and the sacrificial SiGe layers. At this point, the Si sheets are suspended between the S/D epi, supported as well by the inner spacer between sheets. There is a process challenge of completely removing the SiGe in those narrow lateral passages, which poses a corresponding metrology challenge to identify when the SiGe is not fully removed. While line flop over due to aspect ratios and undercuts tend to be the major mechanical challenges faced at the nanoscale, nanowires, and nanosheets run the risk of bending and sometimes collapsing. If the sheets are too thin and/or the width of the trench is too long, this is the process point where the risk is highest. Prior metrology work to characterize bending for nanowires was shown by Levi et al.,[17] Seshadri et al.,[18] and Li et.al[19] report that above ~100 nm gate lengths, sheets will begin to sag due to "stiction," adhesive forces that encourage sheet sticking. Depending on a

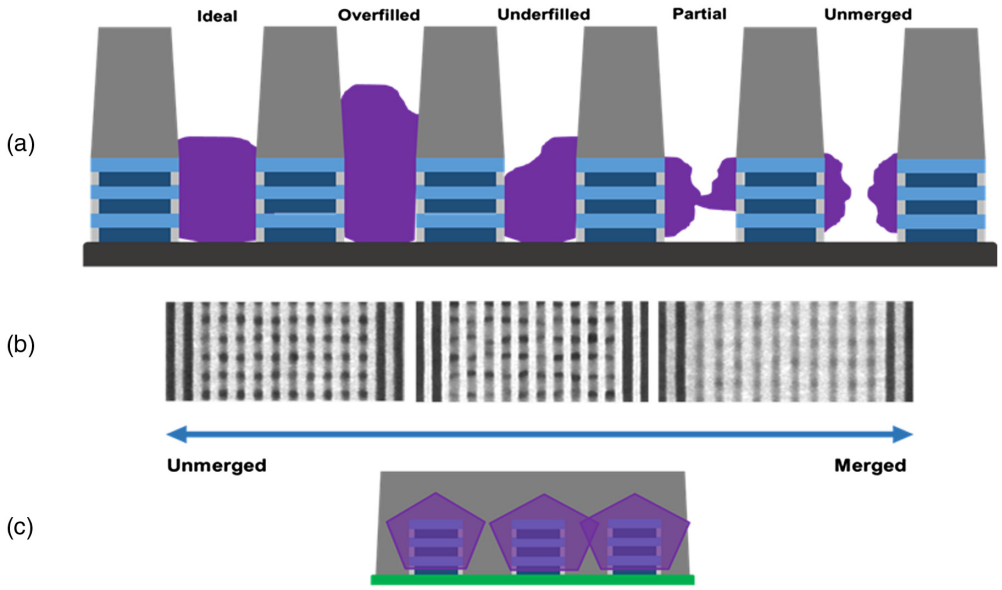

Fig. 3 Schematic of epi growth scenarios that need to be captured by in-line metrology. (a) Epi growth can encounter many non-ideal nucleations and fill states. (b) Merge quality spectrum is a visible top-down with SEM. (c) The origin of unmerged states is depicted by cartoon.[16]

given integration flow and the process assumptions, there are likely design spaces that must simply be ruled out to prevent collapse risk, unless other engineering feats can be accomplished.

Last before the middle-of-line (MOL) stages are the replacement metal gate (RMG) module [Fig. 2(h)]. Here, HK and metal thin films on the order of angstroms are being deposited within the cavities previously occupied by the SiGe sheets. The combination of materials deposited and their thickness are highly influential to the threshold voltage (V_T) options for these GAA devices,[20] so monitoring at this point is also relevant to performance metrics.

3 Critical Modules and Metrology Challenges

It may be clear from the process flow descriptions that at each successive processing stage, metrology challenges for nanosheets will build on each other as the complexity increases. In this section, metrology challenges will be presented by the processing phase, to highlight the critical and often unique measurements that will be needed for each stage. Where challenges will repeat from module to module, only any additional evolutions of the metrology need will be highlighted after the initial description. In-line metrology techniques are the focus of this discussion, but offline techniques will be included where there is no in-line option currently available.

3.1 *Nanosheet Stack Formation*

In the initial steps, when the thin crystalline Si and SiGe sheets are being grown epitaxially, wafers are still unpatterned. The critical measurements of interest are the individual layer thicknesses and the Ge concentrations for each of the SiGe sheets. Additionally, characterization of the thin film and interface quality, as well as defect density, are desired. Monitoring and controlling thickness, composition, and crystal quality down to the atomic scale are key for optimum device performance since the alternating multilayer film stack will define channel dimensions and electrical characteristics.

Non-destructive in-line characterization of individual sheet thicknesses in addition to Ge contents can be achieved by high-resolution x-ray diffraction (HRXRD) ω–2θ scans around the (004) Bragg reflection, for example. Additionally, asymmetric (113) reciprocal space maps (RSMs) can be acquired to confirm pseudomorphic growth of the SiGe sheets. One of the main disadvantages of the HRXRD measurements is the acquisition time, which limits economical in-line metrology of ω–2θ scans to only very few locations per wafer. Moreover, the acquisition of RSMs can take hours per location and hence is not a suitable monitoring technique for a manufacturing line. Therefore, a faster solution is desired that allows for dense across wafer sampling. Optical metrology techniques such as ellipsometry and scatterometry have the required speed but optical models must be developed that can account accurately for Ge content and thickness, and are robust enough to avoid parameter correlations between individual layers.[21,22] Depending on the complexity of the multilayer stack, this can become very difficult, particularly, if minute strain variations affect the dielectric functions and interface effects contribute to the optical response. To get started with dense and rapid in-line metrology, an optical technique that is not sheet-specific but yields good results may be set up with much less effort (Fig. 4). The recent introduction of in-line Raman spectroscopy enables a fast and accurate measurement of the Ge composition and allows direct access to the strain of the SiGe layers.[12] Both parameters can be independently determined based on the energy positions of the Si-Si and Si-Ge optic phonon modes, for example. However, a depth-dependence response is difficult to obtain. Here, a hybrid approach or optical metrology in conjunction with machine learning is a possible path to accurate sheet-specific and fast in-line metrology.

As nanosheet technology continues to mature and finer process adjustments are made to further improve device performance, more advanced characterization may be required. Even a very small defect density effects, the crystalline quality will impact carrier mobility and thus device performance. Dislocation etches can be used to determine defect densities but are cumbersome.[23] Further studies are needed to determine the sensitivity of in-line techniques to crystalline dislocation defects, which may have rare occurrences. Other destructive techniques such as scanning transmission electron microscopy (STEM) and precession electron diffraction

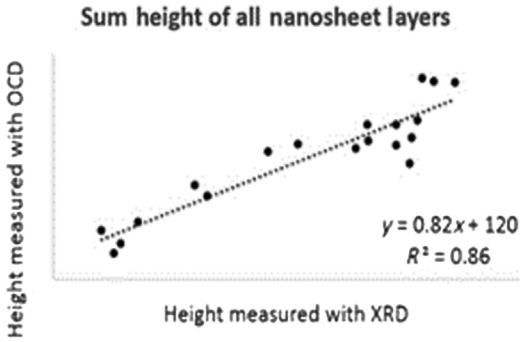

Fig. 4 Comparing scatterometry and XRD measurements for total nanosheet stack height show that both techniques can complete this measurement though scatterometry is less sensitive.[21]

can serve as reference techniques to characterize individual layer thicknesses, SiGe strain, SiGe composition, and interface quality.[19] Additionally, the rate of Ge diffusion from the SiGe sheets into the Si sheets with processing temperatures is challenging but must be understood. Secondary ion mass spectrometry (SIMS) has historically been a standard offline metrology option for composition profiling through a stack, and a paper by Mertens et al.[24] shows the diffusion of Ge via SIMS profiles and high-angle annular dark-field STEM. Bringing SIMS to the suite of in-line options for nanosheet stack monitoring may be necessary as further refinements and controls are required. Then as patterning begins, strain and composition may evolve so methods that are capable of measuring both blanket and patterned structures, such as Raman spectroscopy, are highly beneficial.

3.2 *Fin Patterning*

While the key message in the previous section was focused on individual sheet thicknesses, once patterning begins, the target shifts to individual sheet widths. Traditional top-down critical dimension scanning electron microscopy (CDSEM) continues to be broadly leveraged at all process steps, particularly during patterning, and plays a key role in being a fast, flexible measurement. A challenge is that the bottom width is no longer the only critical dimension (CD) to be captured, and CDSEM likely cannot provide the individual sheet widths which vary due to the fin's sidewall profile, without some additional enhancements. Perhaps through a combination of hybrid metrology, tilted SEM, and advanced algorithms or imaging, all of which could help expand visibility to sidewalls, CDSEM could be able to continue expanding into the three-dimensional space. This is an area where further exploration and calibration are needed. Scatterometry, also known as optical critical dimension (OCD) metrology, can also be employed to model the entire fin geometry at this step,[19] though the correlations between the repeating Si and SiGe sheets may also be an issue for sheet-specific measurements post patterning. Depending on the development stage, the optical model may require either some simplifications, assumptions, or input from other techniques to develop a hybrid solution. Atomic force microscopy has been shown capable of characterizing complex features at decreasing nodes[25] through continued development of new scan modes and could serve as reference metrology for faster model-based techniques. However, sheet-differentiation along the sidewall for sheet-specific width extraction is currently out of reach for this technique.

Two other critical measurements of this nanosheet patterning step are the LER and LWR,[26] as these will increase local variation in sheet widths. LER and LWR have been derived historically from a CDSEM-based measurement, with power-spectral density (PSD) analysis providing a set of parameters to describe the frequency domains and edge characteristics.[27] In recent years, the concept of unbiased LER/LWR[28] as a more accurate measurement of line roughness has been adopted across the industry, as well.

Increased attention to line roughness has improved the available analyses and industry alignment, but sidewall roughness (SWR) continues to be less frequently studied, perhaps because there is no straightforward method for sidewall characterization. SWR may impact LER, where surfaces are very rough, especially given the known weakness of CDSEM metrology for

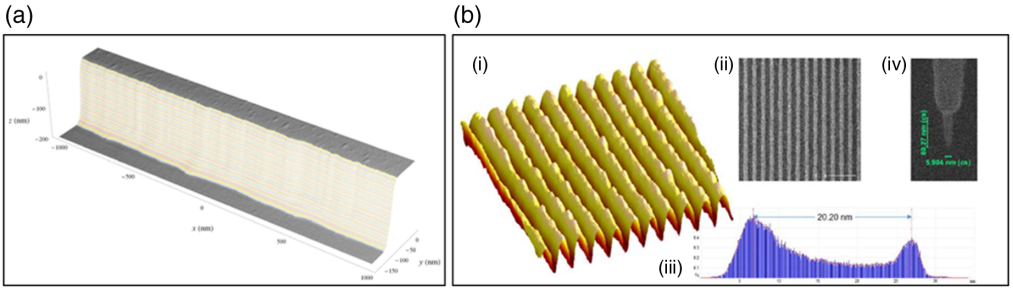

Fig. 5 (a) AFM sidewall profile image developed from scanning the probe parallel to the line for PSD characterization of the sidewall edge roughness.[29] (b) Nanosheet technology's migration to EUV drives smaller dimensions and more challenging AFM metrology. The yellow image (i) is an AFM three-dimensional scan of EUV resist, also shown in the top-down SEM image (ii). The AFM scan is accomplished with the probe shown in (iv).[30]

undercut profiles. But to date, no methodology has been developed to decouple the two contributions. Kizu et al.[29] presented an AFM-based method for PSD LER extraction for sidewalls, and Fig. 5(a) is a three-dimensional representation of the AFM scans derived from scanning parallel to the sample to acquire the sidewall surface profiles for PSD analysis. The method was not available as an in-line technique and was also demonstrated on features larger than typically required for nanosheet devices, such that this method would be difficult to translate to relevant product dimensions.

For resist characterization, results from Schmidt et al.[30] showed that AFM may be able to differentiate sidewall profiles well enough without operating in CD-AFM mode where profiles are more tapered. Scans use a very thin AFM probe to characterize this resist and generate three-dimensional plots of the data, shown in Fig. 5(b). Critical dimension small-angle x-ray scattering (CDSAXS), a type of transmission SAXS, may be able to provide some sensitivity to SWR, but currently, there is no good reference metrology. There are also challenges to bringing CDSAXS in line with product-friendly specifications, specifically for throughput, signal-to-noise ratios, and spot sizes that allow for patterned wafer measurement pads.

Tied to the CD and LER/LWR measurements are some other process monitoring methods. Local CD uniformity (LCDU) also needs to be considered during fin module metrology discussions, as patterning considers shifting from optical lithography to EUV.[18] Direct EUV-printed fins expand the design space, and while not quite a technical challenge, this drives more metrology which adds both time and cost to any learning cycle. LCDU is typically an aggregation of CDSEM measurements, but recent papers by Kong et al.[31] and Schmidt et al.[32] have shown that LCDU and LER may be extracted by scatterometry in conjunction with machine learning approaches. Figure 6 shows that LCDU results are very well matched and with a tight distribution, through different resists and process stages, for both CDSEM and scatterometry-based techniques. LCDU characterization by scatterometry could improve the time and cost of in-line monitoring, especially when coupled with the more traditional measurements for geometric parameters mentioned above. For process flows with multi-patterning solutions instead of EUV, pitch walk metrology solutions that were popularized for the finFET node will need to be revisited for nanosheet fins.[33]

3.3 *Dummy Gate, Spacer, and Inner Spacer*

Measurements surrounding the gate patterning and spacer/inner spacer modules will have many of the same challenges as fin patterning—CD, roughness (line and sidewall), and LCDU. Through all these steps, the tall dummy gate is present, which for tight gate pitches increases the challenge for any technique that requires line of sight or is limited to surface-level characterization. When EUV is used for direct gate patterning rather than self-aligned double patterning or self-aligned quadruple patterning (SAQP), more metrology time is required to fully characterize all variations within the relevant design space. Profile variability can also become more prominent as the feature space broadens. Figure 7 from Seshadri et al.[26] shows an example,

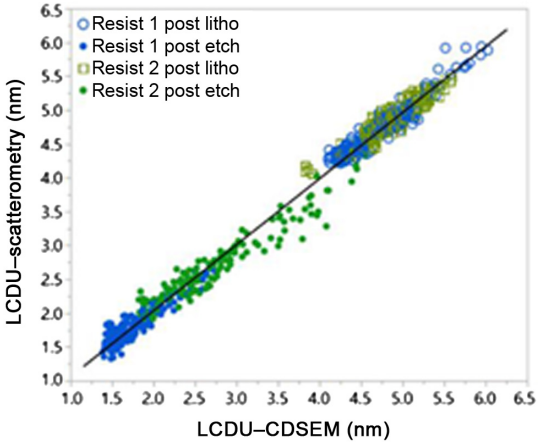

Fig. 6 Comparison of LCDU for post lithography and post etch via using two different resists. The chart compares data obtained by machine learning-assisted scatterometry and traditional CDSEM metrology.[31]

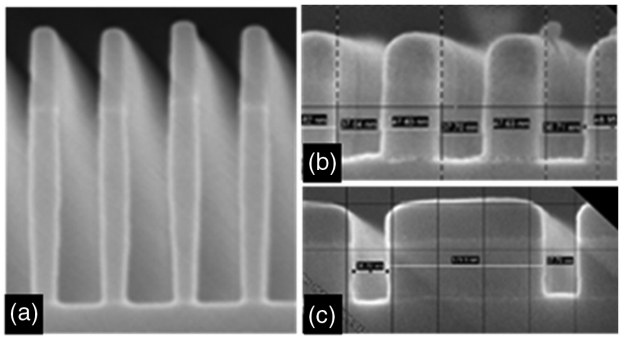

Fig. 7 TEM cross-sections of features with different line aspect ratios that were patterned at the same EUV lithography step. The three images show profile variation can occur due to etch effects from wider EUV-enabled aspect ratio ranges: (a) sub-50 nm pitch and (b and c) >100 nm pitch.[26]

with the undercut narrow lines on the left, while the wider aspect ratio features on the right have more consistent vertical sidewalls. Top-down techniques like CDSEM are generally blind to this effect, so a broad sampling plan is possible but likely would not be sensitive to this kind of variation. Model-based metrology techniques like scatterometry need to anticipate the profile change in the model to parameterize accordingly and have enough models with varying designs to capture the change through a pitch.

Indent characterization for the sacrificial SiGe sheets has drawn a majority of metrology discussion at this part of the flow due to its role in setting device parameters and the impact that many of the other parameters discussed to this point have on the process. Due to the complexity of the resulting structure, model-based techniques can have dozens of material and geometric parameters to solve for, which can make both a robust and very flexible parameter set challenging. However, this is perhaps the most critical step for sheet-specific metrology, as each sheet dimension impacts the performance of the device and deviations can induce a variety of failures at subsequent processing steps.

There have been several published studies on the ability of techniques like scatterometry and CDSAXS to solve for the average indent depth. Korde et al.[34] show CDSAXS is capable of distinguishing indent depth and profile for a nanowire test structure through the indent and inner spacer steps [Fig. 8(a)]. The SAXS beamline at the Argonne National Lab was used for this study, and previous work was performed by a team using the same beamline to explore advancements required for in-line sources leveraging finFET geometries.[35] There is, however, no published work thus far showing the capability of existing in-line SAXS systems to solve for these kinds of nanosheet applications. Scatterometry accounts for a majority of the in-line results on

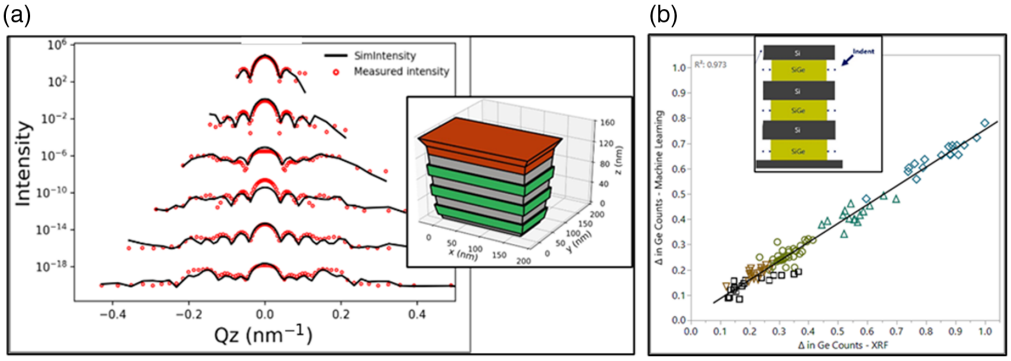

Fig. 8 (a) CDSAXS intensity fringes can be translated to different nanowire indent depths and show sensitivity to etch variations in nanowire test structures.[34] (b) The difference in Ge counts measured by XRF before and after the inner spacer etch correlates to the indent depth. By coupling XRF as a reference data set with scatterometry data, a machine learning model can be trained. The chart shows the ML model tracks well with XRF.[36]

indent monitoring. Kong et al.[36] describe a hybrid solution combining Ge counts from low-energy x-ray fluorescence (LE-XRF) with scatterometry to develop a machine learning (ML) solution for indent monitoring, which was shown to be sensitive to different etch conditions [Fig. 8(b)]. Building on this, Schmidt et al.[37] show a pathway to sheet-specific indent measurements using a combination of spectral interferometry, which leverages scatterometry, and XRF counts. More development in this area is expected, given the importance of sheet-specific characterization.

After the SiGe sheets are indented, the conformal inner spacer is deposited which fills the indent and then is trimmed back so only the Si sheets are exposed on the sidewall in the nanosheet region. Monitoring the inner spacer width and coverage on the dummy gate is important for multiple reasons. Once an ideal indent is achieved, as discussed in the previous paragraph, the inner spacer needs to fully fill this indent to ensure the gate length after channel release. The only existing in-line option to characterize the spacer width and coverage on device-like structures is a scatterometry-based model that is flexible enough to capture the possibilities for variation. As the indent step was already challenging enough, there may be a possibility to fix some of the variables using the prior measurement results in a feed-forward manner. Or a hybrid metrology approach might reduce the parameter space, for example using XRF to solve for Ge count difference and relying on scatterometry to map counts to indent depth plus interpret the rest of the structure. These are possibilities based on the published work for different metrology solution methods, but applying these strategies to these specific structures would require development and validation.

3.4 *Epi Growth*

Patterned epi nucleation and growth can be a difficult step to monitor, as it has many more variables compared to a spacer deposition or other non-patterning steps. Here, epi is intended to be nucleating selectively on the exposed Si sheets only, then growing and merging to fill the trench entirely. Shifts in the epi process that change the growth rates or behavior or unintended epi growth on random nucleation need to be captured in metrology solutions.

There have been a few metrology studies presented addressing some areas of consideration for this module. Kong et al.[38] described methods to characterize the density of epi defects called "nodules" and to localize them along with the height of the dummy gate [Fig. 9(a)], which can help identify the root cause of the defect. These solutions required a combination of CDSEM, scatterometry, and machine learning to achieve these two results, but Fig. 9(b) shows the power of hybrid metrology to achieve a measurement that was previously qualitatively attained through offline cross-section characterization.

An AFM-based study by Breton et al. focused on the epi height characterization and merge quality.[16] Average epi height may be determined via scatterometry on metrology macros or

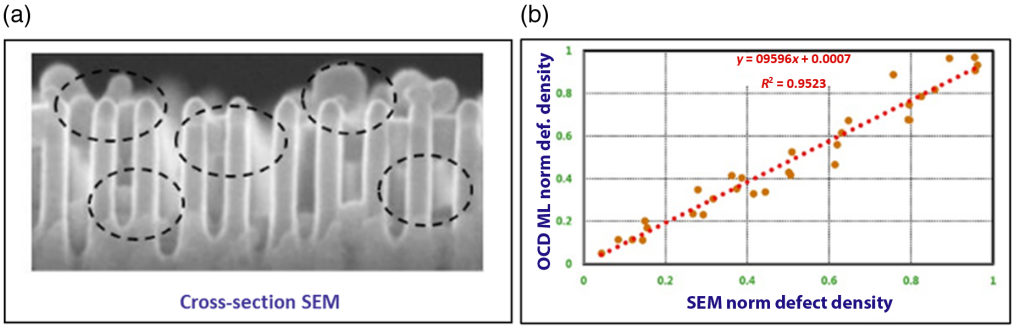

Fig. 9 (a) Epi nodules can form anywhere within the trench between dummy gates or on top of the dummy gates, as shown in the TEM image. (b) Using top-down SEM imaging to calculate defect density as reference metrology for a machine learning model, scatterometry can be used to measure the defect density.[38]

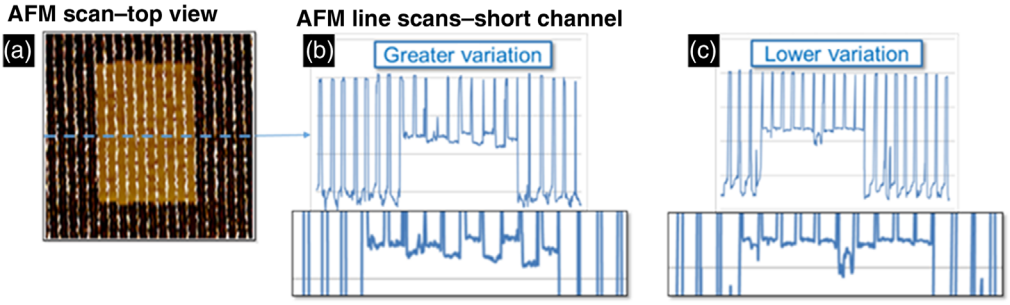

Fig. 10 (a) A set of AFM line scans from a top-down perspective, where the lighter color in the center represents the epi-filled trenches and the darker outside are the non-epi trench regions; the light vertical line features are the dummy gates. (b) and (c) AFM line scans extracted from the device regions with epi are shown. The line scans show examples of high and low epi variation, with zoomed-in clips from the epi surface.[16]

device regions that are larger than the spot size, but variations in the epi height and local measurements on device macros would not be possible. Tilt SEM may provide some visibility to the variation, and future work may show a path to utilize this capability for epi height monitoring. For direct measurement of the epi height, AFM offers a path forward, as shown in Fig. 10. Patterns with trenches larger than 50 nm are easily characterized by existing AFM probes and methods, but on-device measurements require innovation as trench dimensions shrink below probe widths and maintain a relatively high aspect ratio. While this applies to earlier patterning stages for nanosheets as well, the epi module is where this demonstrated capability may be most beneficial. By characterizing the variation of the height, the measurement can also provide feedback on the epi merge quality, another important metric for this module.

A remaining metrology challenge for epi growth is identifying when all the nanosheet sheets are not fully connected, through incomplete nucleation or growth. Height monitoring may catch when the top sheet is not connected, but the bottom sheet's connectivity is hidden from any top-down techniques and essentially there is a void at the bottom of the trench. Previous work has been completed with machine learning and a hybrid solution of scatterometry and XRF to detect voids in metal lines,[39] but a related epi-stage solution has not been published, to the authors' knowledge. A similar machine learning model with extensive reference metrology would be required to develop a qualitative readout (i.e., some defectivity vs. widespread defectivity), and the eventual solution will continue to blur the line between defect inspection and metrology.

3.5 *Channel Release*

The sacrificial SiGe sheets are finally etched during the channel release module, and as previously discussed, this step requires metrology to both identify when SiGe is not completely

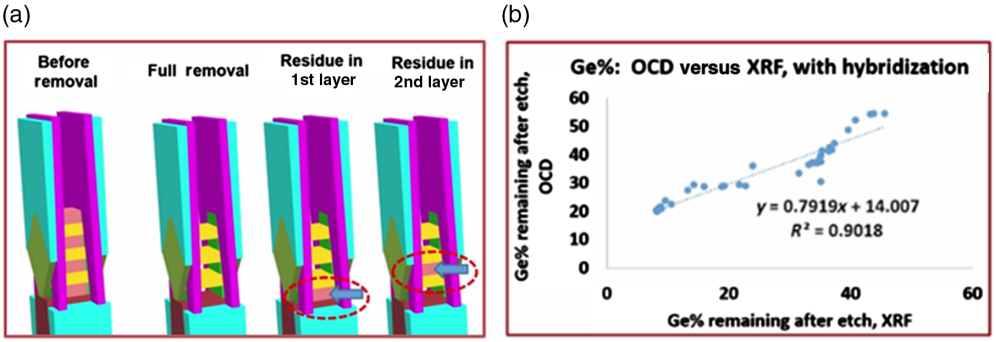

Fig. 11 (a) Schematic illustrates where residues may remain after the sacrificial sheets are removed. (b) A correlation plot of Ge residue from hybrid OCD and XRF metrology, which can then enable a model-based readout of where the residues are located.[40]

removed and also to flag when the suspended Si sheets sag due to mechanical instability or stiction. It is also possible the etch could alter the sheet dimensions, so the sheet thickness after removal is the third measurement of interest. Scatterometry again has a large role and must be sensitive to both the resulting geometry of the cavity and any remaining Ge. As the unit cell geometry is still very complex, Muthinti et al.[40] demonstrated that continued use of machine learning and reference metrologies like XRF may be required to develop a robust solution for residue localization and characterization at this step (Fig. 11). While strain metrology was not identified particularly in earlier sections, it would be especially important at channel release to monitor how the strain has evolved after removing the SiGe sheets via Raman metrology.[12,41]

In the epi section, it was stated that bottom sheet connectivity to epi is a gap for metrology/defect inspection solutions currently. After channel release, the connectivity can now be looked at directly through the sheets, rather than the epi. A prior study shows some opportunity via a classic defect detection method, voltage contrast, to identify when top sheets are not fully connected,[42] but it still has the same top-down challenge where bottom sheet visibility is obscured. By filtering out secondary electrons below the energy spectrum peak in the SEM signal, the contrast change can indicate when the top sheet is not connected, as shown in Fig. 12. Perhaps a future method where tilt SEM[43] is combined with voltage contrast would provide visibility to each sheet's connectivity. This could also potentially point to broken sheets, as they would no longer be connected, but voltage contrast would likely not have sensitivity to sagging sheets, which would still retain the connection to the S/D epi.

Detecting sagging sheets is still an open metrology challenge, which currently is best identified through the cross-section. The hybrid AFM scan and CDSEM image of sagging sheets in Fig. 13 were completed on a cross-sectioned and flipped nanowire,[17] so in-line methods to do the same analysis are still in need. Through the pairing of reference cross-sections and machine learning, perhaps some very small signals can be detected from optical or x-ray-based techniques

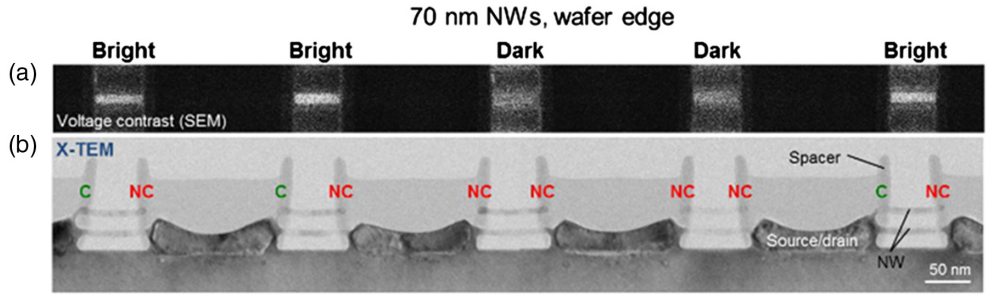

Fig. 12 Detecting voltage contrast during SEM imaging for a two-sheet nanosheet structure can identify shorts between nanowires and S/D epi. (a) Example SEM image with contrast varying for the sheets and (b) corresponding cross-section of sheets showing connected (C) and not connected (NC) sheets.[42]

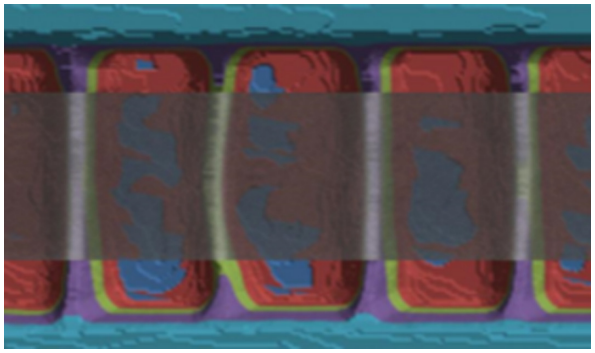

Fig. 13 Image formed by overlaying an AFM topographic scan (colored outer regions) and CDSEM tilted SEM image (center grayscale region) of the same cross-sectioned nanowire structure to detect and measure wire buckling.[17]

which could point to stiction or mechanical failures. This is another case where sheet-specific results may be necessary.

3.6 *Replacement Metal Gate*

The last nanosheet-specific module before entering MOL and back-end processing is the RMG module. It is defined by the deposition of multiple thin-film materials, which are conformal to the Si sheets and the other exposed surfaces. These film thicknesses are on the order of angstroms to single nanometers, so a highly sensitive and accurate measurement is required, and this needs to be applied to all dimensions to characterize the top, bottom, and sidewall thicknesses. Device performance would be compromised when a given film is so thick as to merge in the channel and prevent another film from wrapping around each sheet. A scatterometry solution may be capable of a single-step measurement, but a more robust solution may be reached by combining scatterometry with a technique like an x-ray photoelectron spectroscopy (XPS). In a study by Vaid et al.,[44] hybrid metrology utilizing XPS's angstrom-level sensitivity and scatterometry's geometric strengths to characterize a conformal thin film over fin structures with varying aspect ratios. Figure 14 shows the improvements in accuracy for the patterned fin structure using the hybrid solution over XPS alone, relative to a reference XPS dataset on a planar target.

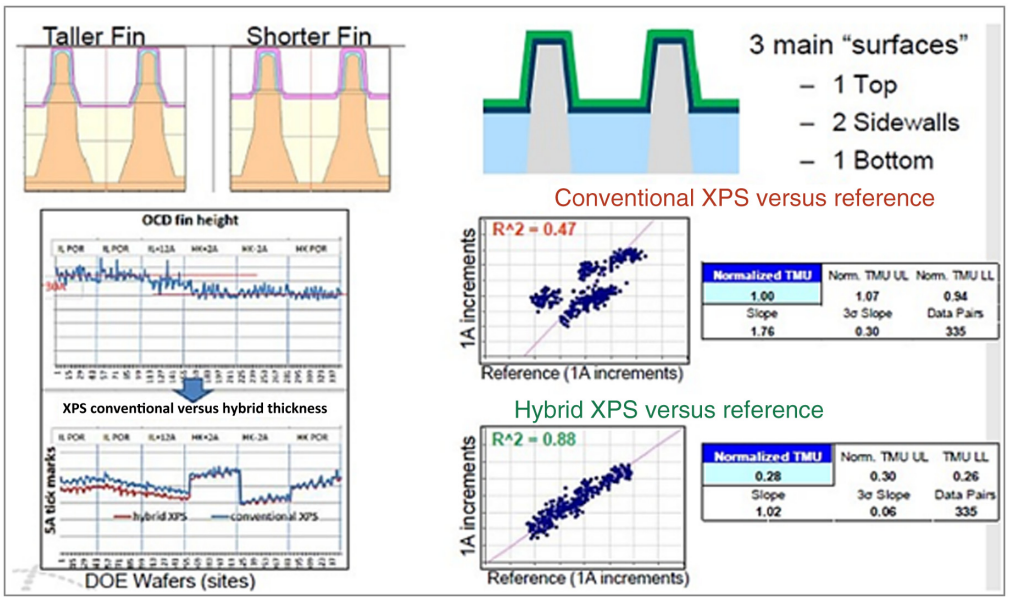

Fig. 14 Robust three-dimensional thin films metrology requires XPS hybridization with a geometry-focused technique to resolve angstrom scale sensitivity on non-planar structures.[44]

3.7 *Module Review: Metrology Capabilities and Needs*

The current best-known metrology methods and challenges per module have been described in the prior subsections, and Table 1 consolidates that review. Future metrology needs point to improvements in throughput and sensitivity, support for increasingly small dimensions, and more reference metrology. There is also a general need for new methods for process monitoring to be in-line and non-destructive. Specifically, improvements with regard to sheet-specific characterizations are required throughout the FEOL processing steps.

4 Metrology Opportunities

After reviewing the critical FEOL nanosheet modules from both the processing and metrology perspectives, it should be clear that there are many synergistic challenges and opportunities. A pervasive theme is that these increasingly complex structures cannot be fully measured with one technique alone–creative combinations to maximize each technique's strengths does provide

Table 1 Current metrology solutions and future non-destructive needs by module.

Module	Measurement	Current metrology	MAM speed	Future metrology needs
Si/SiGe stack formation	Sheet thickness	XRD	Slow	Faster sheet-specific measurements
	Sheet composition	XRD	Slow	Improved sensitivity to crystalline defects
		Raman	Fast	
	Crystal quality	XRD, RSM	Slow	
	Strain	Raman	Fast	
Fin patterning	Sheet width (CD) and uniformity (CDU)	CDSEM	Fast	
		OCD	Fast[a]	
	Fin LER and LWR	CDSEM	Fast	
		AFM	Slow	Sub-30 nm trench solution
	SWR	AFM	Moderate	Sub-30 nm trench solution
	Fin height	OCD	Fast[a]	
		AFM	Moderate	
Dummy gate, spacer, and inner spacer	Sheet width (CD) and uniformity (CDU)	CDSEM	Fast	
		OCD	Fast[a]	
	Dummy gate LER and LWR	CDSEM	Fast	
		OCD	Fast	
		AFM	Slow	Sub-30-nm trench solution
	SWR	AFM	Moderate	Sub-30-nm trench solution
	Gate profile	OCD	Fast[a]	
	Sheet indent	OCD	Fast[a]	Sheet-specific sensitivity on targets with gate
		XRF	Moderate	
	Inner spacer residues	OCD	Fast[a]	Sensitivity down to monolayer residues on channels
	Inner spacer thickness	OCD	Fast[a]	Improved sheet-specific sensitivity

Table 1 (*Continued*).

Module	Measurement	Current metrology	MAM speed	Future metrology needs
Epi growth	Epi fill height	OCD	Fast[a]	
		AFM	Moderate	
	Epi volume	Raman	Fast	
	Epi composition and quality	Raman	Fast	
	Merge quality	SEM	Moderate	Further calibration for quantitative versus manual readouts
		AFM	Moderate	Improved sensitivity to buried nucleation issues and voids
	Unintended nucleation	OCD Inspection	Fast[a] Fast	In-line, non-destructive reference for *Z*-location of nodules
Channel release	Sacrificial layer residues	OCD XRF	Fast[a] Moderate	Improved sensitivity to residues and sheet-specific detection
	Sheet thickness	OCD	Fast[a]	Sheet-specific development
	Epi connectivity	VC-SEM	Fast	Sensitivity verification for 3+ sheets
				Sheet-specific development
	Sheet sagging detection	TEM	—	Non-destructive, in-line development
RMG	Thin film thickness Other geometric parameters	XPS OCD	Moderate Fast[a]	Sheet-specific development

[a]MAM time for OCD is fast, but the optical model development time (time-to-solution) is variable based on structural complexity

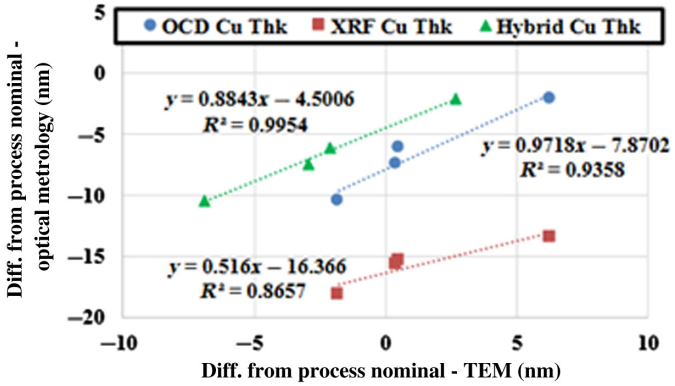

Fig. 15 Accuracy of the thickness (height) measurement for copper-filled metal lines using OCD or XRF alone can be improved by combining it into a hybrid measurement. The hybrid solution that either technique can provide on their own.[45]

value and will continue to be important. X-ray and scatterometry measurements have proven to be a very strong pairing through study after study, given their complementary material and geometric sensitivities. Figure 15 depicts an example where copper lines post-CMP were measured by scatterometry and XRF. The results show that with hybrid metrology, the accuracy and precision of the measurement relative to the TEM reference data can be improved.[45] Combining techniques also provides an opportunity to leverage more niche metrologies which may

Table 2 Record of ML use in the Metrology Conference at the SPIE Advanced Lithography Symposium.

Year	SPIE AL: Metro ML sessions	Papers w/ML or deep learning in title or abstract	Total papers	%
2017	0	2	89	2
2018	2	10	90	11
2019	1	13	98	13
2020	1	17	86	20
2021	0	20	107	18

otherwise be rather engineering-focused due to throughput or complexity. Equipment vendors have also embraced this path, providing increasingly powerful software packages to take advantage of all the data produced by their tools, in addition to increasing the number of signals a single piece of equipment might be able to detect.

Machine learning itself deserves attention, as over the past 5 years it has seen a tremendous level of adoption in the semiconductor industry. Its capabilities are being developed for imaging, analysis, and prediction, and its potential in these areas has been realized through many research works. Metrology is entering a new era of expanded sensitivity to fingerprints and nuances in signals, data, and trends, with an opportunity for reduced time to detection. In the SPIE Advanced Lithography Metrology, Inspection, and Process Control conference, machine learning was just being introduced in 2017.[46,47] As Table 2 shows, the number of sessions devoted to machine learning jumped to two sessions in the following year as the community saw a huge rise in its use. Then machine learning continued to provide a session-worth of material for 2 years before becoming pervasive enough that it no longer warranted its own session in 2021. In the past 2 years, about one-fifth of all published papers within this conference contained "machine learning" or "deep learning" either within the tile or the abstract. Correlations, regression analysis, and complex mathematical models are not new to metrology or the industry, but machine learning has accelerated and enhanced existing capabilities.

Algorithm development, integrated into existing software packages, and scalability of compute power through the cloud or more efficient servers have provided the impetus for machine learning's broader adoption. Information Technology (IT) offerings have also advanced to offer systems that can handle increasingly large volumes of data from many sources and provide better recommendations for decision points through data mining and algorithms. There have been publications through all these years detailing the evolution of manufacturing controls that leverage metrology data, including control loops like the system described by Ren et al.[48] for SAQP pitch walk control. A smart and predictive control system that accounts for all the potential metrology variables discussed in the previous sections would certainly need to leverage some of these software and data-analysis advancements to gain insights in real time.

Little attention has been given in this review to a classic technique, overlay, due to the heavy reliance on process-driven evolution of features, rather than many interlocking patterning steps. But this does not minimize future opportunities for overlay as it will still play a key role to enable functional patterning of ever-shrinking device features and improve yield across the wafer. Depending on the integration scheme, optical, immersion, EUV, and high-NA EUV single or even multi-patterning lithography steps may all need to be matched in a single process flow. Specifically, when high-NA EUV lithography is entering the mix later this decade, half-field printing effects need to be considered and appropriate process control methodologies developed to maintain minimum on-product overlay.[49] Ongoing trends to study both optical kerf overlay and in-die device overlay through SEM-based techniques are necessary to understand how a wide design space enabled by EUV patterning could create variation between these two methods. Machine learning cannot be forgotten here either, as there are many signals and parameters to take advantage of, so variation can be captured, understood, and removed.[50]

5 Conclusion

Through this paper, the FEOL nanosheet process flow has been described in-depth, along with the process challenges that require metrology solutions. Nanosheets are the next main architecture for the logic industry, but innovations that were developed in the finFET era will continue to be valuable for nanosheets. Nanosheet stack metrology from blanket deposition through patterning and processing requires more advanced and nuanced measurements like strain through Raman or angstrom-level sheet-specific thicknesses through ellipsometry or scatterometry to isolate impacts to devise performance. Enhanced hybridization options and understanding to leverage geometric and material sensitivities are available. Roughness metrology has a common language, and scatterometry continues to increase in prevalence for its strengths characterizing buried features and complex three-dimensional parameters. In-line SAXS tools exist on the market and have been shown in offline studies to measure the more challenging nanosheet process steps, but these systems need to show good SNR, improved throughput, and small enough spot sizes to be truly in-line capable. SIMS is a traditionally offline measurement with proven data with a nanosheet stack but has just started the migration in-line. Raman spectroscopy has also recently made the jump from offline to in-line, in time for the strain monitoring needs of nanosheet.

There is also a continued opportunity at many process points for inspection and metrology to cross-over, detect, and measure when variations like residues or incomplete epi nucleation occur. Additionally, there is a potential for offline characterization to merge with metrology, bringing increasingly sensitive three-dimensional learning and control to the line. Detecting sagging or broken sheets below the top sheet has no demonstrated solution. And while sheet-specific measurements are the current challenge for model-based techniques, the next challenge would naturally then be to develop a metric to understand the sheet variations within a device array or between dummy gates. Finally, solutions that can detect electrical failures or predict electrical metrics through in-line metrology sooner than later will be of high value as the number of process steps between substrate and packaging continues to increase.

There will be inevitable continuity in the new process developments to enable improvements in nanosheet performance, in the scaling paradigm that this architecture introduces. Plenty of corresponding opportunities for innovation and re-imagining of metrology, inspection, and characterization exist and will arise out of these development cycles, and advancements made will inevitably be instrumental for the future generations of devices and semiconductor processing, as well.

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