JOM Journal of Optical Microsystems

RESEARCH PAPER

Adaptive strategies for uLED wafer-level package and fan-out integration on 12-in. substrate

Chin-Ta Wu,[a,b] Ching-Shih Tsou,[a] Shing-Han Li,[a] and Jeffery Chiang[b,*]
[a]National Taipei University of Business, College of Business, Taipei, Taiwan
[b]Powertech Technology Inc., Hsinchu, Taiwan

ABSTRACT. As semiconductor wafer process technology advances, there is a notable miniaturization of complementary metal-oxide-semiconductor transistors, allowing for a higher transistor density on the predominant 12-in. silicon wafers. Despite this trend, a significant number of applications remain tethered to legacy wafer sizes such as 8 in., 6 in., or even smaller. Economically packaging these devices presents a challenge. Furthermore, many of these applications necessitate that the active surface remains exposed to external environments, contrasting with conventional packaging methods that shield the active surface with epoxy molding compounds. Addressing these specialized needs, we introduce a "chip-first face-up wafer-level fan-out packaging." This innovative approach ensures that the active surface remains outward-facing and accessible for intended interactions with the environment while concurrently enabling electrical connections from the chip to the board on the side opposite to the active surface through the meticulous combination of redistribution layers and through-silicon vias.

Keywords: wafer-level packaging; uLED chip packaging; through-silicon vias

Paper 24017G received Jul. 17, 2024; revised Nov. 19, 2024; accepted Dec. 16, 2024; published Jan. 6, 2025.

1 Introduction and Contextual Background

In the realm of integrated circuit (IC) packaging, the process often centers on separating individual chips from wafers and positioning them onto dedicated substrates. For devices built upon complementary metal-oxide-semiconductor (CMOS) technology, the 12-in. silicon wafer has become the predominant wafer size due to its capacity to support nanoscale transistor fabrication on a massive scale to achieve the economic effect. This has cemented the semiconductor industry firmly within a 12-in. framework. However, specialized applications such as micro light-emitting diode (uLED), micro-electro-mechanical-systems (MEMS) sensors and actuators, and radio frequency largely adhere to 4″ or 6″ wafer dimensions, a reflection of the specific constraints of their fabrication technologies.

Portable consumer electronics, the primary application for these devices, demand low power consumption, compact form factor, and affordability. Traditional packaging often sees chips separated from their parent wafer and set on a laminated substrate. Connections between the chip and substrate are typically achieved via wire bonding or flip chip bonding, with substrate-to-board connections using a ball grid array. Notably, the laminate substrate incurs significant costs, both financially and in terms of board space. Conventional substrate-based packaging methods such as wire-bonding ball grid array (BGA) or flip-chip BGA do not align with the compact demands of portable devices.

*Address all correspondence to Jeffery Chiang, jefferychiang@pti.com.tw

Wafer-level packaging is an approach growing in prominence in portable gadgets such as smartphones and wearables. It sidesteps the need for a laminated substrate, leveraging a redistribution layer (RDL) that is developed at the wafer level using iterative processes of sputtering deposition, lithography, and electroplating.[1–3] In addition, in the field of portable consumer electronics, there existed another application that utilized wafer-level packaging: CMOS image sensor (CIS); however, unlike other devices, such as processors or memory chips, the packaging of CIS required the active side exposed, instead of being encapsulated. This specialized requirement spurred the development and utilization of through-silicon vias (TSVs) to allow the aforementioned RDL to be formed on the backside of the chip to allow both the electrical connection and the sensor side facing upward.[4–11] Although this shrinks the form factor, this wafer-level processing technology induced compatibility issues as most modern wafer-level packaging is tailored for 12-in. wafers, leaving smaller-sized wafers unsupported by many packaging service providers.

The solution is a wafer-level fan-out technique where wafers are initially diced and then situated on a glass carrier, making the process indifferent to the original wafer size.[12,13] There remains, however, the unique needs of certain applications where the active surface must remain exposed for interaction with the environment beyond the confinement of the packaging [see Figs. 1(c) and 1(d)]. This necessitates the use of TSVs. The integration of TSVs further underscores the importance of wafer-level fan-out; without standardizing on a 12-in. glass carrier, non-conformant wafer sizes would struggle to find compatible TSV and RDL machinery.

By incorporating TSVs, pathways are established for electrical connections between the active and reverse sides of the wafer. Through the described RDL process, we present a specialized version of the wafer-level chip scale package, enhanced with TSV [see Fig. 1(c)]. This design promotes a compact form factor, cost efficiency, reduced power consumption, and crucially, the unique feature underlined in this paper: a mass-producible process flow for the active surface to remain exposed for environmental interaction, while providing robust reliability and cost-benefit.

In this report, we also used a uLED wafer, with pixel array and ulens fabricated on the wafer, which at the system level assembly will be mounted on a circuitry board and connected with a controller IC to perform the intended display function.

2 Methods: Technical Details

2.1 Wafer Reconstitution

In the chip-first wafer-level fan-out approach, wafer reconstitution takes precedence before establishing interconnections. Initially, the parent wafer is segmented into individual chiplets. These

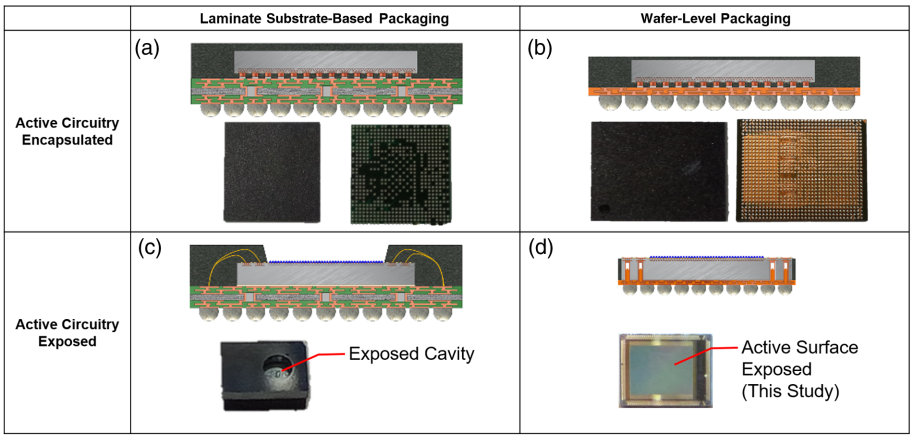


Fig. 1 Comparison of different packaging architecture. (a) a conventional flip chip-chip scale package (FCCSP) where a chip is bonded to a laminate substrate and encapsulated by molding compound, (b) a fan-out wafer level package, where the redistribution layer (RDL) are responsible for chip to board signal connection, (c) a laminated substrate packaged chip with its active surface exposed by a cavity in molding compound, to allow interaction with the outside environment, and (d) a wafer level package where the active surface are facing toward the environment and the electrical connections are re-routed from the active surface to the bottom by the combination of through silicon via (TSV) and RDL.

chiplets are then picked and positioned onto a 12-in. glass carrier with the assistance of a die bonding machine. Our choice of glass as a carrier is strategic, owing to its adjustable coefficient of thermal expansion, which offers the ability to control warpage, which in the realm of wafer-level packaging, if left unchecked, could lead to process-ability issues. To facilitate this, the glass surface is layered with a sacrificial release film followed by a consistent adhesive layer to bond the chiplets securely [see Figs. 2(a) and 2(b)].

Posting the pick-and-place procedure, the next step is the molding process with the epoxy molding compounds (EMCs); in the realm of semiconductor packaging, the EMC serves as an encapsulation that packages the IC and provides protection from the mechanical and chemical influence of the outside. The molding process also introduces a mold flow that may push the bonded chiplets radially, which necessitates the aforementioned adhesive layer. This is succeeded by wafer-level grinding, honing down to either the chiplets' back side or a predetermined chiplet thickness. Once this grinding phase concludes, the wafer reconstitution is complete [see Figs. 2(c) and 2(d)], resulting in what we term the "reconstituted wafer" or simply "recon wafer," now prepared for the TSV and RDL processes.

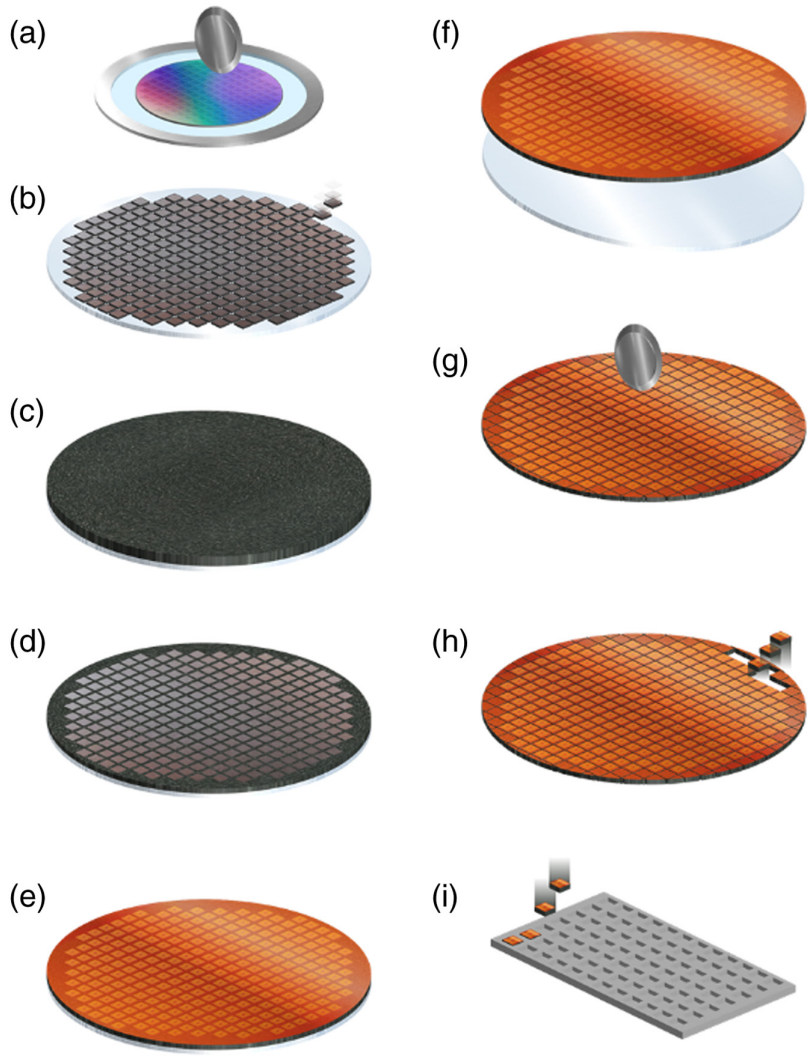


Fig. 2 Process flow of the proposed package design. (a) uLED wafer dicing process, singular the wafer into individual chips, (b) the singulated chips are pick and placed on a glass carrier, forming a reconstituted wafer, (c) the reconstituted wafer is over molded, (d) then grind the mold surface until the revelation of the silicon chips, (e) TSV and RDL fabrication process are performed on the exposed chips, (f) the glass carrier is debonded, (g) singulation of the reconstituted wafer into individual packaged uLED chips, (h) the chips are picked up, and (i) then put into chip tray, ready for shipping

The crux of wafer reconstitution lies in its ability to transform parent wafers of varied dimensions into a standardized 12-in. format, ensuring universal compatibility with a broad spectrum of wafer-level process machinery.

2.2 TSV on Recon Wafer

The formation of TSVs is achieved through a series of carefully orchestrated steps. The process begins with lithography to earmark areas designated for TSVs. The photoresist was coated onto the recon wafer, then followed by the exposure to define the pattern, and finally with the assistance of the development process. The defined pattern will have its photoresist removed, with the other unexposed area still coated with the photoresist. As the photoresist is coated on the back side of the wafer, a stepper equipped with an infrared camera was used to properly align with the mark on the front side. Prior to the lithography step, we measured the post-molding die shift, and the die shifted radially from the center where the dies further from the center will have a greater shift. From Fig. 3, we can see that the maximum shifts measured are <10 μm, where the TSV landing pad design is 80×80 μm, where the diameter of the TSV itself is 30 μm, meaning that the TSV pattern will land within the boundary across the entire wafer. This allowed the stepper machine to use global alignment, without the need to individually align to each and every die and therefore greatly increase the throughput. This is followed by a dry etching technique, vertically penetrating the silicon until it reaches the landing pad on the active side of the chiplet. The previous lithography step ensures that the dry etching process only removes the silicon from the defined area and leaves the rest of the area protected by the photoresist intact. To ensure the purity and integrity of the TSV, a wet-dry-wet procedure is employed to purge polymer byproducts, resulting from dry etching, from both the TSV hole base and its sidewalls. Upon thorough cleaning, chemical vapor deposition (CVD) deposits a thin silicon oxide layer, serving as an insulating liner for the TSV. This liner is pivotal, averting potential current leakage.

Introducing TSV dry etching on a recon wafer is a groundbreaking step, veering away from the industry's conventional approach where chiplets were pre-equipped with TSVs within their parent wafer, pre-reconstitution. Our methodology caters to specific application wafer sizes, which traditional TSV machinery struggles to accommodate. The recon wafer emerges as a solution, making TSV formation feasible for these unconventional wafer sizes.

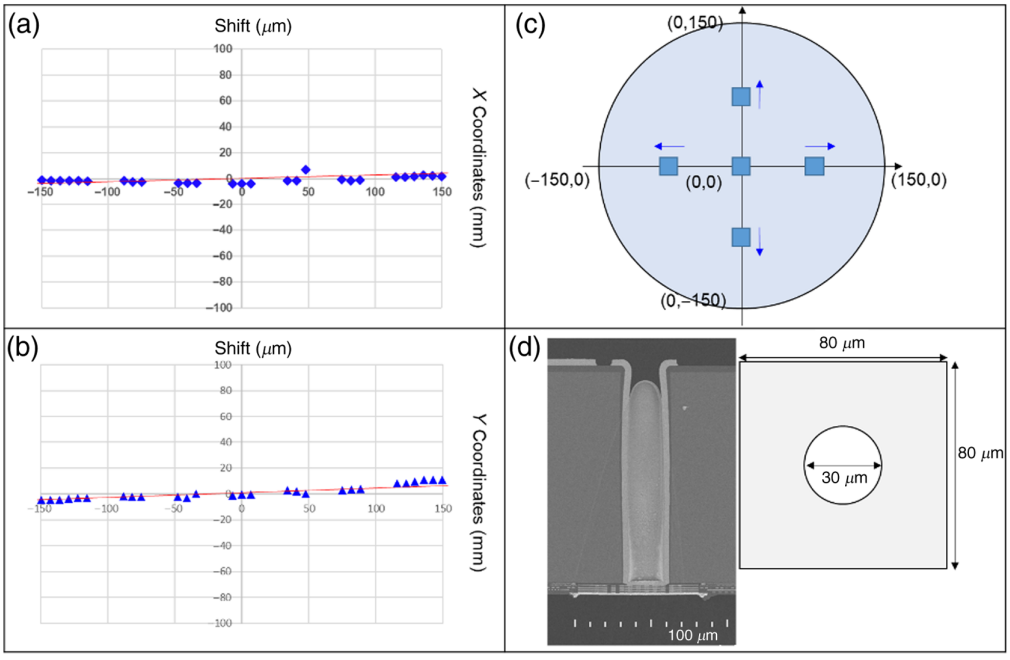


Fig. 3 Die shift measurement result, both panels (a) and (b) showed <10-μm shift, and panel (c) identifies the direction of the shifts. Panel (d) shows the design and dimension of the TSV hole and landing pad; as long as the shift is below 25 μm, the TSV will be able to land within the pad.

However, utilizing TSVs on a recon wafer is not without challenges. Early in our development, we observed adverse interactions between the TSV gas mixture and the molding compound, leading to chamber contamination. In such tainted environments, TSV dry etching could result in the formation of undesirable "TSV spikes" at the hole's base. These spikes pose a threat as they evade coverage by the liner oxide, rendering the TSV prone to current leakage and subsequent electrical malfunctions.

To counteract this, our research led us to employ low-temperature silicon oxide as a hard mask. This effectively insulates the TSV etchant gas from the molding compound. This hard mask not only seals off the molding compound but also offers a protective shield during the wet–dry–wet cleaning process. Here, the "dry clean" denotes a plasma ashing procedure, which without the hard mask, could damage the molding compound and further contaminate the chamber. The reason why we deposited the silicon oxide under low temperature (100°C) is to avoid the undesired outgassing from the molding compound, which like another vacuum process such as TSV dry etching, will contaminate the chamber, leading to machine repair costs.

After the TSV and RDL fabrication processes, the processed recon wafer is now singulated once again to form the individually packaged chiplets. They are then picked and placed onto a tray or other packing material, now ready for the next hierarchy of the electronics assembly process [see Figs. 2(g)–2(i)].

2.3 Finished Package

The finished package (see Fig. 4) demonstrated a significantly reduced form factor as compared with another design, which used wire bond interconnection to a laminate substrate. The current industry standard front end-of-line process necessitates that the active circuitry and the chip-to-board interconnection terminals be manufactured on the same side of the wafer, without TSVs, which will require using conventional wire bonding technique to form chip-to-board interconnection while maintaining the active side of the chip facing the environment. The wires also necessitated the need for a larger footprint beyond the uLED chip's boundary to allow interconnection. The wafer-level-processed TSVs and RDLs removed the need for a laminate substrate and wires, the EMC no longer needed to cover the loop height of the wires to provide protection, and the absence of a laminate substrate decreased the area needed for the package. These combined reductions resulted in significantly reduced form factor in both Z height and XY area (97% and 42%, respectively, excluding the balls). As the targeted application is consumer AR devices, where the device appearance needs to be socially acceptable and portable, this reduction in form factor is critical to achieving this purpose, where the device is very space-constrained and electrical components need to be miniaturized to relinquish the much-needed space for the on glasses battery. The wafer-level fan-out process introduced in this paper also demonstrated consistent >99.8% electrical test yield (open/short test).

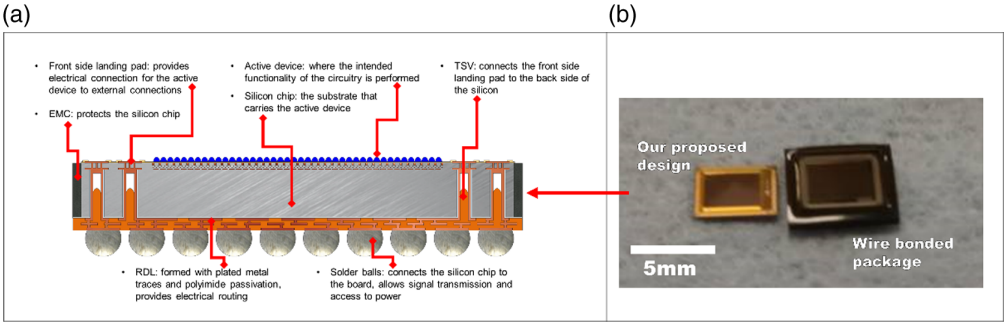


Fig. 4 Finished package of our proposed design and its features. The wire-bonded package uses the same uLED chip that is interconnected to a laminate substrate; the wires are embedded in epoxy. (a) the key compositions of the proposed wafer level package design, the combination of TSV and RDL on the uLED chip allows great reduction in form factor, (b) form factor comparison of the proposed design and a wire bonded package which contained a chip of similar size.

3 Result: Reliability Assessment

3.1 Pre-reliability Assessment and Process Improvement

All electronics must undergo a reliability verification process to determine the end product's mean time to failure and ensure that it is adequate for its intended life cycle under normal use.

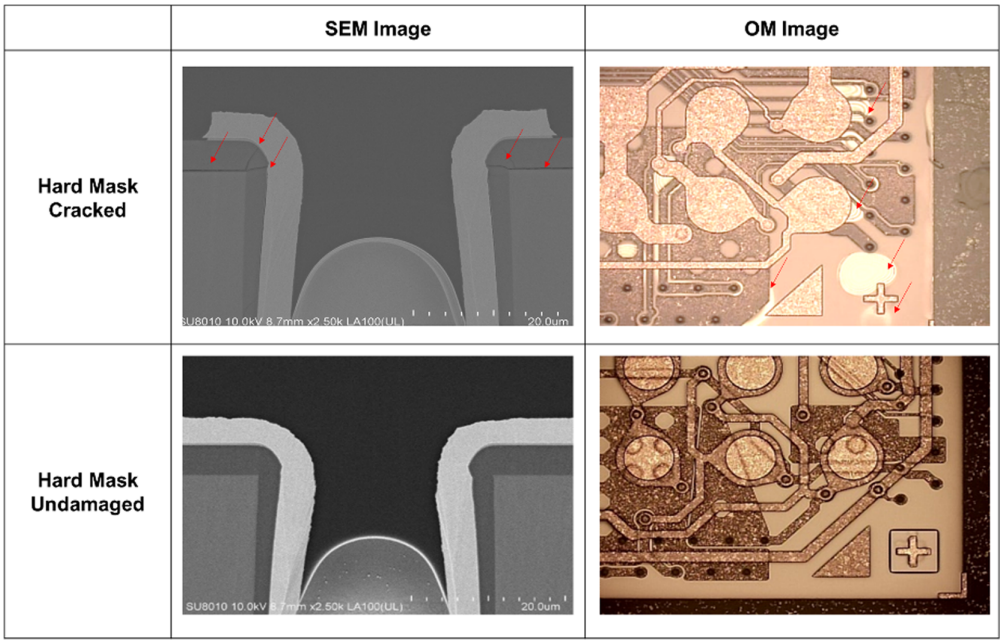
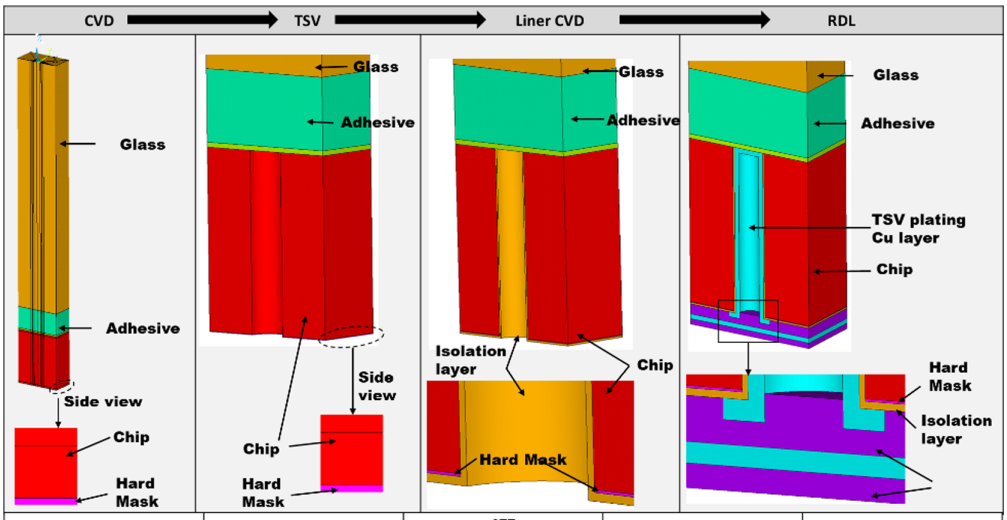


Fig. 5 Comparison of hard mask integrity after the pre-reliability assessment.



Material	Young's Modulus (MPa)	CTE (ppm/C)	Tg	Poisson's Ratio
DAF	303 (30C) 373 (100C) 443 (170C) 473 (200C) 533 (260C)	130/390	88	0.3
Silicon Chip	112000	2.6	-	0.28
SiO_2	73000	0.55	-	0.17
Cu	95000 (30C)	17	-	0.35
Glass	74800	3.2	-	0.238
Si_3N_4	31000	2.3	-	0.24

Fig. 6 Simulation model and input parameters.

When we first developed the packaging structure, we subjected the packaged samples to multiple reflows.

After the assessment, all packaging structures were observed to be intact, except for the hard mask. Post multiple reflow tests (three times reflow with a peak temperature of 260°C), we observed hard mask delamination around the TSV region (see Fig. 5). Cross-section analysis revealed that the delamination propagated toward the interior of the TSV, leading to liner oxide cracks. These cracks and delamination could lead to reliability failure around the joint of the TSV and RDL, causing electrical failure. We deduced that the root cause was the brittle nature of the selected oxide material, SiN, and the stress introduced upon the SiN layer during the TSV etching process, causing the SiN material around the TSV hole to succumb to the stress and delaminate from the silicon surface, further leading to the cracking of the liner oxide around the upper neck of the TSV.

To mitigate this issue, a new material needed to be developed. We studied other CVD deposition materials and performed finite element modeling (ANSYS) to perform stress simulations using our proposed packaging structure to emulate the stress buildup around the TSV hole during our process. Package structure and process parameters were input into the model (see Fig. 6), and the results are shown in Fig. 7, indicating a 5% reduction in stress if we adopt silane oxide (leg 1) as a hard mask instead of our POR SiN (leg 2). We have also performed unit warpage simulation (Fig. 8) with the silane oxide (leg 1) and POR SiN (leg 2) as hard masks. The simulation result also points out that SiN as a hard mask does lead to a 5% greater warpage than the silane ox. The simulation results of film stress and unit warpage both indicate that the silane oxide, owing to its

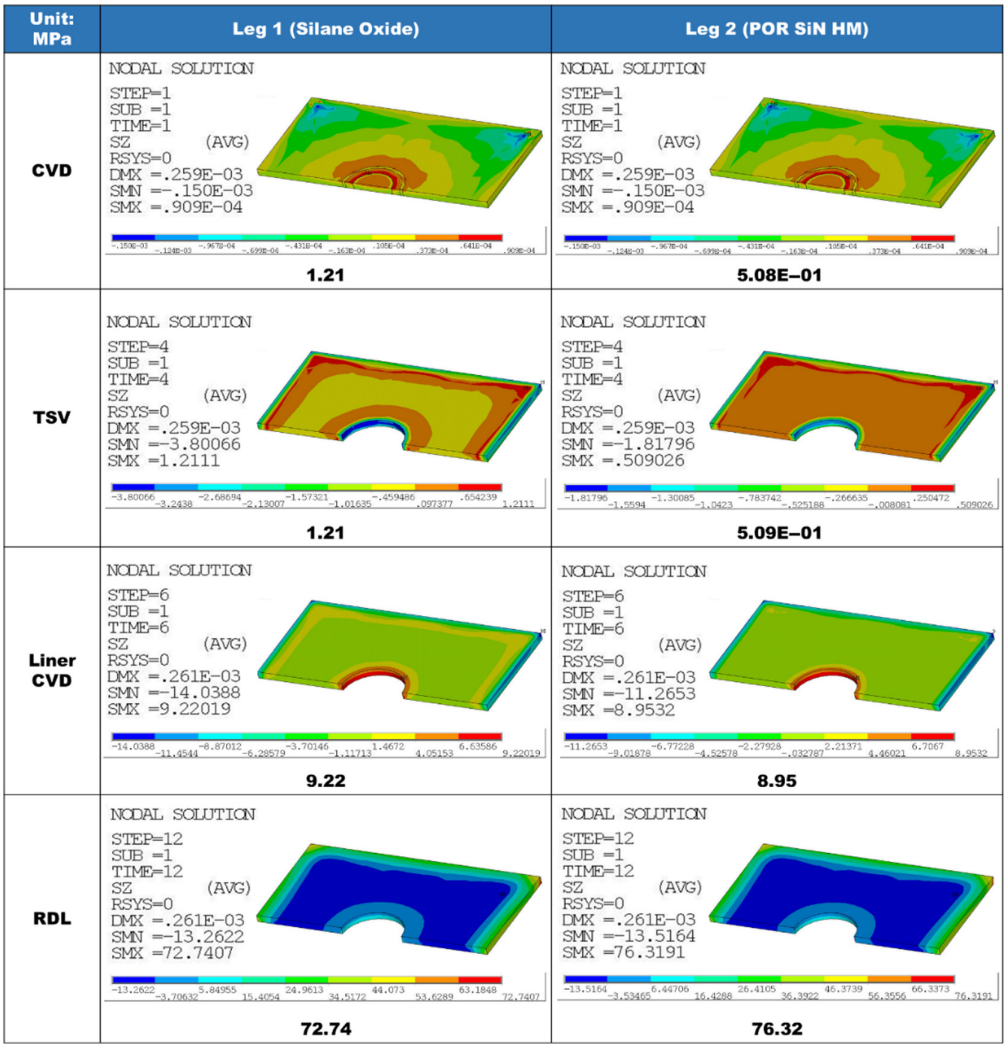


Fig. 7 Stress simulation result of TSV region by process stage.

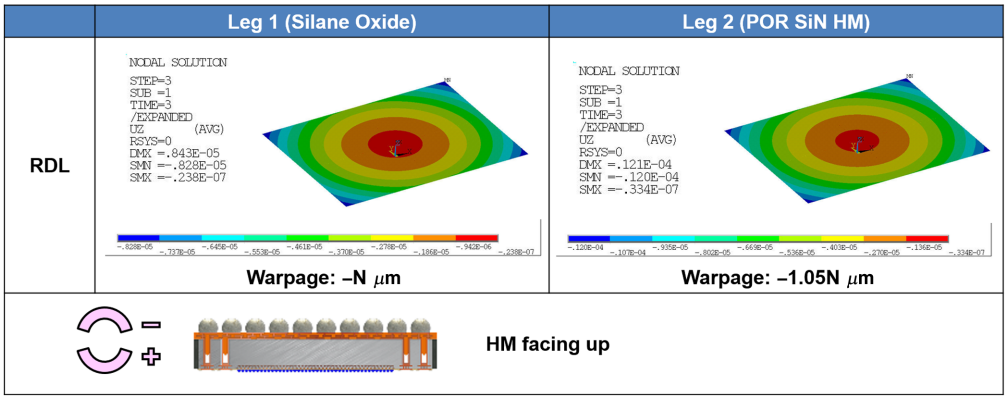


Fig. 8 Warpage simulation result of chip units after the RDL process.

lower modulus, does induce smaller warpage, and therefore, a smaller warpage induced stress, making it a potential candidate to replace the SiN material to avoid the delamination issue that we observed. We fabricated another batch to empirically prove the robustness with the same pre-reliability procedure.

The efficacy of switching from SiN to silane oxide was 100% effective, with no delamination or cracks observed after the multiple reflow tests. Now, the structure is fit for the formal reliability test.

Table 1 Matrix of reliability items and results.

Reliability item	Condition	Sample size	Readout	Result
Precon	Bake (120'C, 24 h)	24ea	After soaking	24/24 pass
	MSL4, 3x reflow (245'C)			
	Soak 196 h, 30'C/60% RH			
TCT	Condition-B	10ea	250 cycs	10/10 pass
	–55'C~+125'C		500 cycs	10/10 pass
			1000 cycs	10/10 pass
uHAST	Condition-A	10ea	168 h	10/10 pass
	110'C/85% RH, 33.3psia		264 h	10/10 pass
HTS	125'C	10ea	500 h	10/10 pass
			750 h	10/10 pass
HTHH + Baking 85'C 3 h	45'C/90% RH	10ea	100 h	10/10 pass
			200 h	10/10 pass
			300 h	10/10 pass
			400 h	10/10 pass
			500 h	10/10 pass
HTHH + Baking 85'C 3 h	65'C/90% RH	10ea	100 h	10/10 pass
			200 h	10/10 pass
			300 h	10/10 pass
			400 h	10/10 pass
			500 h	10/10 pass

Fig. 9 Light-on image of the packaged chiplet.

3.2 Formal Reliability Assessment

To evaluate the reliability of the designed package, three lots were fabricated and subjected to reliability assessment. After the reliability trial, the units were subjected to a light-on test to verify the chip's functional integrity. Table 1 summarizes the reliability results, where all three lots passed the component-level reliability tests: Precon, TCT, uHAST, HTS, and HTHH. Figure 9 shows the light-on image of the packaged uLED chip, demonstrating sufficient brightness and good robustness and stability of the designed package. We further conducted SAT and cross-section analyses to ensure no abnormalities.

4 Conclusion

The innovative "chip-first face-up wafer-level fan-out packaging" approach addresses the unique needs of applications requiring exposed active surfaces. By leveraging TSVs and RDLs, our method ensures compatibility with various wafer sizes, enhances package reliability, and reduces form factors, making it ideal for space-constrained consumer electronics such as AR devices. Reliability assessments confirmed the robustness and stability of the designed package, validating its suitability for commercial applications. This research paves the way for further advancements in wafer-level packaging, ensuring that legacy wafer sizes can benefit from modern packaging technologies.

Disclosures

The authors declare that they have no conflicts of interest relevant to this study.

Code and Data Availability

The data that support the findings of this article are not publicly available due to intellectual property concerns. For a deep dive discussion on the technical details, please contact: jefferychiang@pti.com.tw.

Acknowledgments

The authors would like to acknowledge his colleagues in the PTI advanced packaging development team, including the members from R&D, product engineering, process engineering, and integration teams. The authors especially thank Jeffery Chiang, for years of tireless work, and the orchestration of collaboration between cross-functional teams. Moreover, the authors would like to further extend their gratitude to our customer who provided valuable uLED chiplet wafers for the development of this packaging technology.

References

1. D. Yu, "A new integration technology platform: integrated fan-out wafer-level-packaging for mobile applications," in *Symp. VLSI Technol.* (2015).

2. J. H. Lau, "Redistribution-layers for fan-out wafer-level packaging and heterogeneous integrations," in *China Semicond. Technol. Int. Conf. (CSTIC)* (2019).
3. J. Chiang and P. Wu, *Opportunities and Challenges of Heterogeneous Integration: From IC Packaging POV*, SPIE Press, Bellingham, Washington (2023).
4. W. Ping et al., "TSV fabrication for image sensor packaging," in *China Semicond. Technol. Int. Conf. (CSTIC)* (2015).
5. J. Charbonnier, "Wafer level packaging technology development for CMOS image sensors using through silicon vias," in *Electron. Syst.-Integr. Technol. Conf.* (2008).
6. L. Chen, F. Dai, and W. Zhang, "Study on the structure of vertical through silicon via with aspect ratio 2.5:1 for CMOS image sensor," in *Int. Conf. Electron. Packaging Technol.* (2018).
7. T. Matthias et al., "CMOS image sensor wafer-level packaging," in *Int. Conf. Electron. Packaging Technol. and High Density Packaging* (2011).
8. S. Wang et al., "Wafer-level packaging design with through substrate grooves as interconnection for GaAs-based image sensor," *IEEE Trans. Comp. Packaging Manuf. Technol.* **3**, 2022–2028 (2013).
9. Y. Guillou and A.-M. Dutron, "3D IC products using TSV for mobile phone applications: an industrial perspective," in *Eur. Microelectron. and Packaging Conf.* (2009)
10. Y. Wang et al., "Process development of 3D WLCSP for ultra-thin CMOS image sensor," in *Int. Conf. Electron. Packaging Technol. (ICEPT)* (2020).
11. S. Ma et al., "Development and reliability study of 3D WLCSP for automotive CMOS image sensor using TSV technology," in *IEEE Electron. Comp. and Technol. Conf. (ECTC)* (2020).
12. N. Fujimori et al., "Wafer level package by using post dicing process," in *Int. Conf. Electron. Packaging (ICEP)* (2014).
13. T. Braun et al., "Fan-out wafer level packaging for MEMS and sensor applications," in *IEEE Electron. Comp. and Technol. Conf. (ECTC)* (2019).

Chin-Ta Wu is with Powertech Technology Co., Ltd., Hsinchu, Taiwan, where he serves as the senior vice president. He received his BS degree in mechanical engineering from Tamkang University, Taiwan in 1991 and is currently pursuing a PhD at the National Taipei University of Business. His research interests include data science and artificial intelligence applications. He has nearly 30 years of industry experience in semiconductor manufacturing, including production management, process development, and the introduction of big data/AI/IoT technologies.

Ching-Shih Tsou is with the Information and Decision Sciences Institute, National Taipei University of Business (NTUB), Taipei, Taiwan, where he is a professor and director of the Intelligent Control and Decisions Centre. He received his PhD degree. His research interests include machine learning, game theory, evolutionary multi-objective optimization, time series, and reinforcement learning. He founded the Chinese Academy of R Software and established the Data Science and Business Applications Association of Taiwan (DSBA) in 2013.

Shing-Han Li is with the Department of Accounting Information, National Taipei University of Business, Taipei, Taiwan, where he is a professor. He received his MS degree in computer science and information engineering from Tatung University, Taiwan, in 1996, and his PhD in information management from National Chung-Cheng University, Taiwan, in 2006. His research interests include machine learning, computer auditing, service quality control, ERP systems, and information security.

Jeffery Chiang is a department manager in the R&D department at Powertech Technology Inc. (PTI). He holds a master's degree in power mechanical engineering from National Tsing Hua University. With extensive experience in research and development, he leads a team focused on innovative engineering solutions. His expertise in wafer-level packaging has contributed significantly to advancement in the field and the success of PTI's projects.